

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

R8C/2H Group, R8C/2J Group RENESAS MCU

REJ03B0217-0010 Rev.0.10 Jul 20, 2007

1. Overview

1.1 Features

The R8C/2H Group and R8C/2J Group of single-chip MCUs incorporate the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space and is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI. Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

1.1.1 Applications

Electric power meters, electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 **Specifications**

Table 1.1 outlines the Specifications for R8C/2H Group and Table 1.2 outlines the Specifications for R8C/2J Group.

Specifications for R8C/2H Group Table 1.1

Item	Function	Specification			
CPU	Central processing	R8C/Tiny series core			
CFU		Number of fundamental instructions: 89			
	unit				
		Minimum instruction execution time:			
		125 ns (f(XIN) = 8 MHz, VCC = 2.7 to 5.5 V)			
		250 ns (f(XIN) = 4 MHz, VCC = 2.2 to 5.5 V)			
		Multiplier: 16 bits × 16 bits → 32 bits			
		 Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits 			
• C		Operation mode: Single-chip mode (address space: 1 Mbyte)			
Memory	ROM, RAM	Refer to Table 1.3 Product List for R8C/2H Group.			
Power Supply	Voltage detection	Power-on reset			
Voltage	circuit	Voltage detection 3			
Detection		- Comings accounts			
Comparator		2 circuits (shared with voltage monitor 1 and voltage monitor 2)			
Comparator		External reference voltage input is available			
I/O Ports		CMOS I/O ports: 16, selectable pull-up resistor			
	Clock goneration				
Clock	Clock generation	• 2 circuits: On-chip oscillator (high-speed, low-speed)			
	circuits	(high-speed on-chip oscillator has a frequency adjustment function),			
		XCIN clock oscillation circuit (32 kHz)			
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16			
		Low power consumption modes:			
		Standard operating mode (low-speed clock, high-speed on-chip oscillator,			
		low-speed on-chip oscillator), wait mode, stop mode			
		Real-time clock (timer RE)			
Interrupts		External: 3 sources, Internal: 17 sources, Software: 4 sources			
		Priority levels: 7 levels			
Watchdog Time	er	15 bits × 1 (with prescaler), reset start selectable			
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler)			
		Timer mode (period timer), pulse output mode (output level inverted every			
		period), event counter mode, pulse width measurement mode, pulse period			
		measurement mode			
	Timer RB	8 bits x 1 (with 8-bit prescaler)			
	111101112	Timer mode (period timer), programmable waveform generation mode (PWM			
		output), programmable one-shot generation mode, programmable wait one-			
		shot generation mode			
	Timer RE	8 bits × 1			
	THITICI IXE	Real-time clock mode (count seconds, minutes, hours, days of week), output			
		compare mode			
	Timer RF	16 bits × 1 (with capture/compare register pin and compare register pin)			
	1	Input capture mode, output compare mode			
Serial	UARTO, UART2	Clock synchronous serial I/O/UART x 2			
Interface					
LIN Module	I	Hardware LIN: 1 (timer RA, UART0)			
Flash Memory		Programming and erasure voltage: VCC = 2.7 to 5.5 V			
riash wemory		Programming and erasure voltage. VCC = 2.7 to 3.5 v Programming and erasure endurance: 100 times			
		Program security: ROM code protect, ID code check Debug for a first code of the c			
0		Debug functions: On-chip debug, on-board flash rewrite function			
Operating Frequency/Supply		f(XIN) = 8 MHz (VCC = 2.7 to 5.5 V)			
Voltage		f(XIN) = 4 MHz (VCC = 2.2 to 5.5 V)			
Current consur		TBD			
Operating Amb	pient Temperature	-20 to 85°C (N version)			
		-40 to 85°C (D version) ⁽¹⁾			
Package		20-pin LSSOP			
		Package code: PLSP0020JB-A (previous code: 20P2F-A)			
-					

NOTE:
 1. Specify the D version if D version functions are to be used.



Table 1.2 Specifications for R8C/2J Group

ltom	Specifications to	·		
Item	Function	Specification		
CPU	Central processing	R8C/Tiny series core		
	unit	Number of fundamental instructions: 89		
		• Minimum instruction execution time:		
		125 ns (f(XIN) = 8 MHz, VCC = 2.7 to 5.5 V)		
		250 ns (f(XIN) = 4 MHz, VCC = 2.2 to 5.5 V)		
		Multiplier: 16 bits × 16 bits → 32 bits		
		 Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits 		
		Operation mode: Single-chip mode (address space: 1 Mbyte)		
Memory	ROM, RAM	Refer to Table 1.4 Product List for R8C/2J Group.		
Power Supply	Voltage detection	Power-on reset		
Voltage	circuit	Voltage detection 3		
Detection				
Comparator		2 circuits (shared with voltage monitor 1 and voltage monitor 2)		
		External reference voltage input is available		
I/O Ports		CMOS I/O ports: 12, selectable pull-up resistor		
Clock	Clock generation	1 circuits: On-chip oscillator (high-speed, low-speed)		
	circuits	(high-speed on-chip oscillator has a frequency adjustment function),		
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16		
		Low power consumption modes:		
		Standard operating mode (high-speed on-chip oscillator, low-speed on-chip		
		oscillator), wait mode, stop mode		
Interrupts		External: 3 sources, Internal: 14 sources, Software: 4 sources		
		Priority levels: 7 levels		
Watchdog Time	er	15 bits x 1 (with prescaler), reset start selectable		
Timer	Timer RA	8 bits x 1 (with 8-bit prescaler)		
		Timer mode (period timer), pulse output mode (output level inverted every		
		period), event counter mode, pulse width measurement mode, pulse period		
		measurement mode		
	Timer RB	8 bits x 1 (with 8-bit prescaler)		
		Timer mode (period timer), programmable waveform generation mode (PWM		
		output), programmable one-shot generation mode, programmable wait one-		
	Time or DE	shot generation mode		
	Timer RF	16 bits x 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode		
Serial	UART0	Clock synchronous serial I/O/UART x 1		
Interface				
LIN Module		Hardware LIN: 1 (timer RA, UART0)		
Flash Memory		Programming and erasure voltage: VCC = 2.7 to 5.5 V		
•		Programming and erasure endurance: 100 times		
		Program security: ROM code protect, ID code check		
		Debug functions: On-chip debug, on-board flash rewrite function		
Operating Frequency/Supply Voltage		f(XIN) = 8 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 4 MHz (VCC = 2.2 to 5.5 V)		
Current consur	mption	TBD		
	pient Temperature	-20 to 85°C (N version)		
	,	-40 to 85°C (D version) ⁽¹⁾		
Package		20-pin LSSOP		
		Package code: PLSP0020JB-A (previous code: 20P2F-A)		
NOTE:		1		

NOTE:

1. Specify the D version if D version functions are to be used.

1.2 Product List

Table 1.3 lists Product List for R8C/2H Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2H Group. Table 1.4 lists Product List for R8C/2J Group, Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2J Group.

Table 1.3 Product List for R8C/2H Group

Current of Jul. 2007

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212H1SNSP (D)	4 Kbytes	256 bytes	PLSP0020JB-A	N version
R5F212H2SNSP (D)	8 Kbytes	384 bytes	PLSP0020JB-A	
R5F212H1SDSP (D)	4 Kbytes	256 bytes	PLSP0020JB-A	D version
R5F212H2SDSP (D)	8 Kbytes	384 bytes	PLSP0020JB-A	

(D): Under development

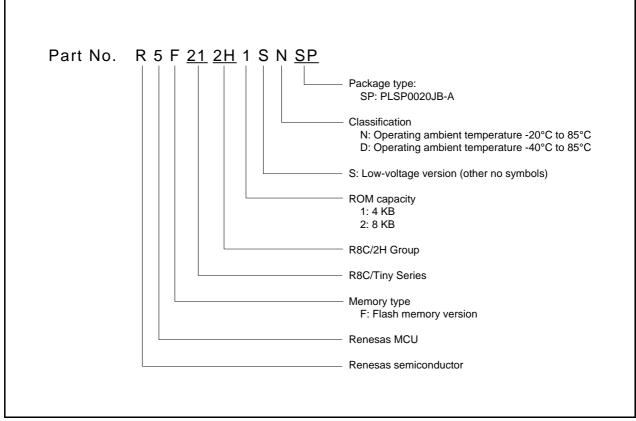


Figure 1.1 Part Number, Memory Size, and Package of R8C/2H Group

Table 1.4 Product List for R8C/2J Group

Current of Jul. 2007

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212J0SNSP (D)	2 Kbytes	256 bytes	PLSP0020JB-A	N version
R5F212J1SNSP (D)	4 Kbytes	384 bytes	PLSP0020JB-A	
R5F212J0SDSP (D)	2 Kbytes	256 bytes	PLSP0020JB-A	D version
R5F212J1SDSP (D)	4 Kbytes	384 bytes	PLSP0020JB-A	

(D): Under development

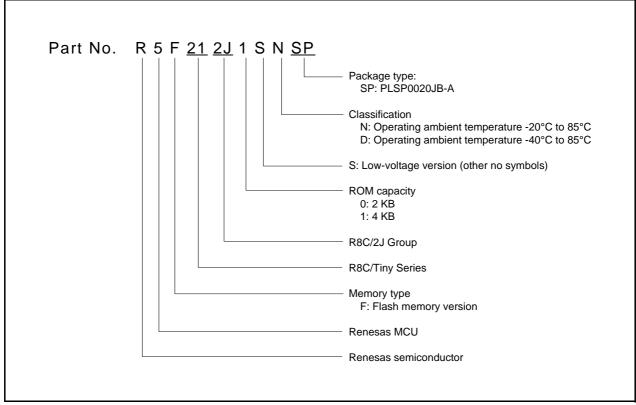


Figure 1.2 Part Number, Memory Size, and Package of R8C/2J Group

1.3 Block Diagram

Figure 1.3 shows a Block Diagram of R8C/2H Group and Figure 1.4 shows a Block Diagram of R8C/2J Group.

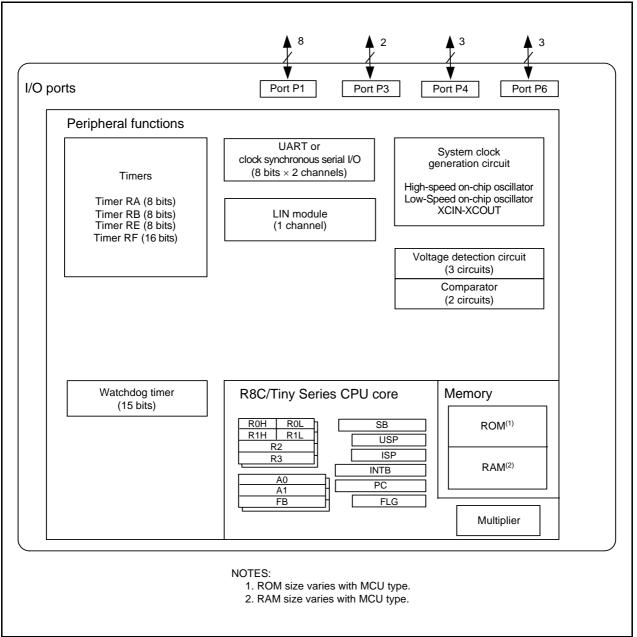


Figure 1.3 Block Diagram of R8C/2H Group

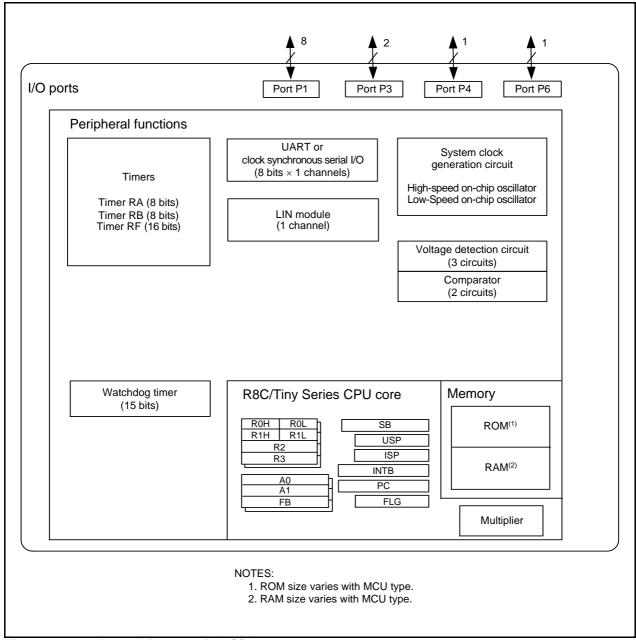


Figure 1.4 Block Diagram of R8C/2J Group

1.4 Pin Assignment

Figure 1.5 shows Pin Assignment (Top View) of R8C/2H Group. Table 1.5 outlines the Pin Name Information by Pin Number of R8C/2H Group.

Figure 1.6 shows Pin Assignment (Top View) of R8C/2J Group. Table 1.6 outlines the Pin Name Information by Pin Number of R8C/2J Group.

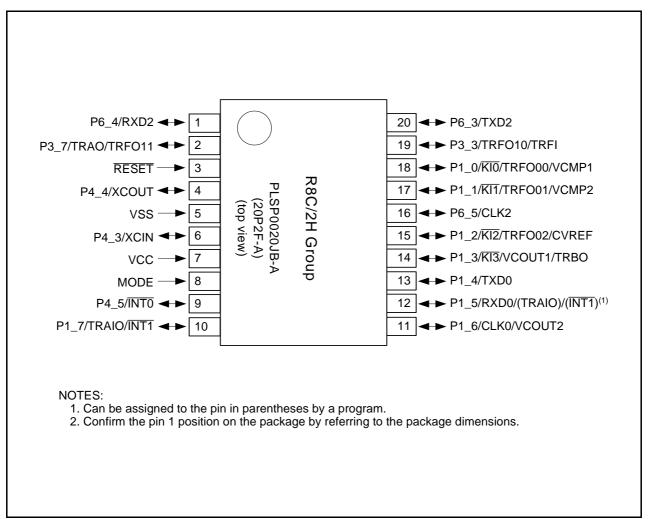


Figure 1.5 Pin Assignment (Top View) of R8C/2H Group

Table 1.5 Pin Name Information by Pin Number of R8C/2H Group

Pin	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
Number	Control Fill	Foit	Interrupt	Timer	Serial Interface	Comparator
1		P6_4			RXD2	
2		P3_7		TRAO/TRFO11		
3	RESET					
4	XCOUT	P4_4				
5	VSS					
6	XCIN	P4_3				
7	VCC					
8	MODE					
9		P4_5	ĪNT0			
10		P1_7	ĪNT1	TRAIO		
11		P1_6			CLK0	VCOUT2
12		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0	
13		P1_4			TXD0	
14		P1_3	KI3	TRBO		VCOUT1
15		P1_2	KI2	TRFO02		CVREF
16		P6_5			CLK2	
17		P1_1	KI1	TRFO01		VCMP2
18		P1_0	KI0	TRFO00		VCMP1
19		P3_3		TRFO10/TRFI		
20		P6_3			TXD2	

^{1.} Can be assigned to the pin in parentheses by a program.

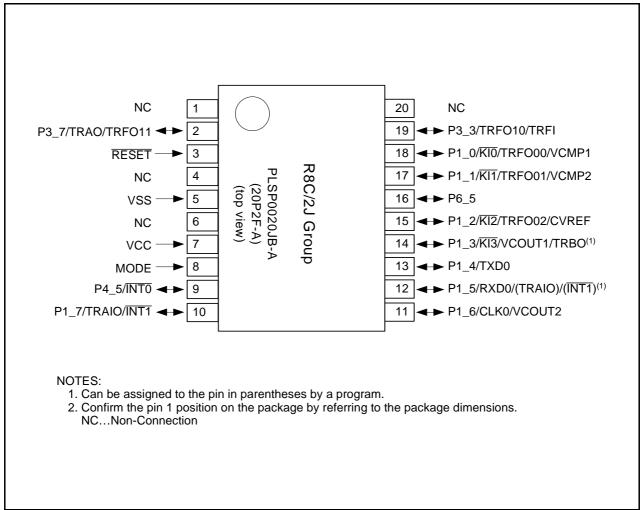


Figure 1.6 Pin Assignment (Top View) of R8C/2J Group

Table 1.6 Pin Name Information by Pin Number of R8C/2J Group

Pin	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
Number	Control Pin	Port	Interrupt	Timer	Serial Interface	Comparator
1	NC ⁽²⁾					
2		P3_7		TRAO/TRFO11		
3	RESET					
4	NC ⁽²⁾					
5	VSS					
6	NC ⁽²⁾					
7	VCC					
8	MODE					
9		P4_5	ĪNT0			
10		P1_7	ĪNT1	TRAIO		
11		P1_6			CLK0	VCOUT2
12		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0	
13		P1_4			TXD0	
14		P1_3	KI3	TRBO		VCOUT1
15		P1_2	KI2	TRFO02		CVREF
16		P6_5				
17		P1_1	KI1	TRFO01		VCMP2
18		P1_0	KI0	TRFO00		VCMP1
19		P3_3		TRFO10/TRFI		
20	NC ⁽²⁾			_		

- 1. Can be assigned to the pin in parentheses by a program.
- 2. NC(Non-Connection)

1.5 Pin Functions

Table 1.7 Pin Functions of R8C/2H Group and Table 1.8 Pin Functions of R8C/2J Group.

Table 1.7 Pin Functions of R8C/2H Group

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	_	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT
XCIN clock output	XCOUT	0	pins. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
INT interrupt input	ĪNTO, ĪNT1	I	INT interrupt input pins
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	0	Timer RA output pin
Timer RB	TRBO	0	Timer RB output pin
Timer RF	TRFI	I	Timer RF input pin
	TRFO00 to TRFO02, TRFO10 to TRFO11	0	Timer RF output pins
Serial interface	CLK0, CLK2	I/O	Clock I/O pin
	RXD0, RXD2	I	Serial data input pin
	TXD0, TXD2	0	Serial data output pin
Comparator	VCMP1, VCMP2	I	Analog input pins to comparator
	CVREF	I	Reference voltage input pin to comparator
	VCOUT1, VCOUT2	0	Comparator output pins
I/O port	P1_0 to P1_7, P3_3, P3_7, P4_3 to P4_5, P6_3 to P6_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.

I: Input

O: Output

I/O: Input and output

NOTE:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 1.8 Pin Functions of R8C/2J Group

Туре	Symbol	I/O Type	Description
Power supply input	VCC, VSS	-	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
INT interrupt input	ĪNTO, ĪNT1	I	INT interrupt input pins
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	0	Timer RA output pin
Timer RB	TRBO	0	Timer RB output pin
Timer RF	TRFI	I	Timer RF input pin
	TRFO00 to TRFO02, TRFO10 to TRFO11	0	Timer RF output pins
Serial interface	CLK0	I/O	Clock I/O pin
	RXD0	I	Serial data input pin
	TXD0	0	Serial data output pin
Comparator	VCMP1, VCMP2	I	Analog input pins to comparator
	CVREF	I	Reference voltage input pin to comparator
	VCOUT1, VCOUT2	0	Comparator output pins
I/O port	P1_0 to P1_7,	I/O	CMOS I/O ports. Each port has an I/O select direction
	P3_3, P3_7,		register, allowing each pin in the port to be directed for input
	P4_5, P6_5		or output individually.
			Any port set to input can be set to use a pull-up resistor or not
			by a program.

I: Input

O: Output

I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

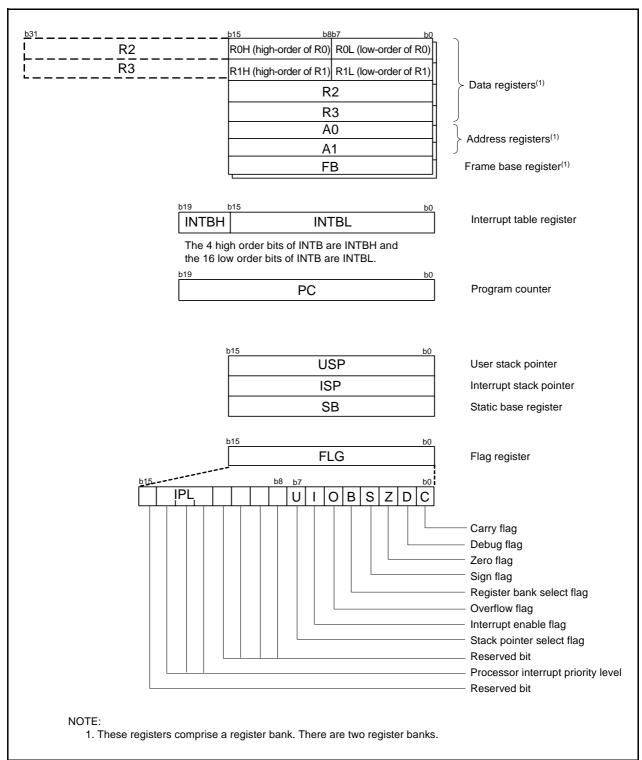


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 **Carry Flag (C)**

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 **Zero Flag (Z)**

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

Figure 3.1 is a Memory Map of R8C/2H Group and Figure 3.2 is a Memory Map of R8C/2J Group. The R8C/2H group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 4-Kbyte internal ROM area is allocated addresses 0F000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 256-bytes internal RAM area is allocated addresses 00400h to 004FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

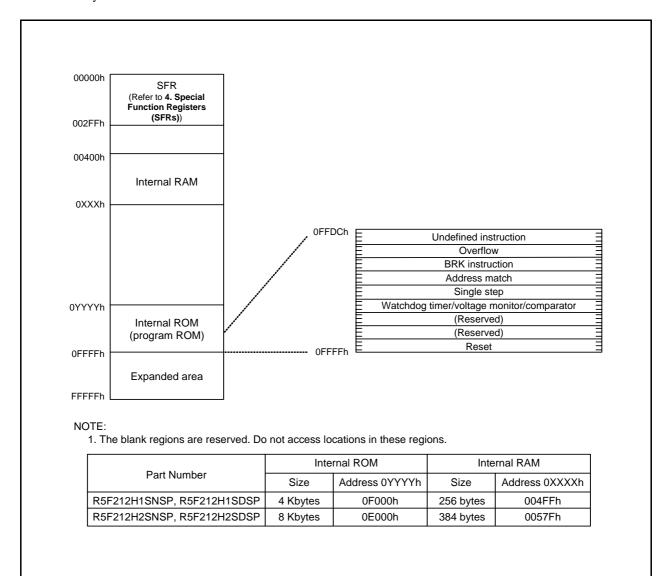


Figure 3.1 Memory Map of R8C/2H Group

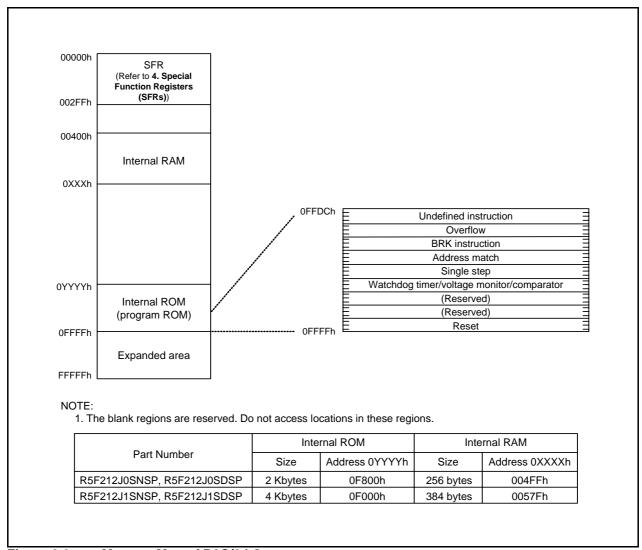


Figure 3.2 Memory Map of R8C/2J Group

Special Function Registers (SFRs) 4.

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

Table 4.1 SFR Information (1)⁽¹⁾

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01001000b
0007h	System Clock Control Register 1	CM1	00h
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	System Clock Select Register ⁽³⁾	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽²⁾
001Dh			
001Eh			
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
0024h			
0025h			
0026h			
0027h			
0028h	Clock Prescaler Reset Flag ⁽³⁾	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch	5 1 2 F 2 2 2 2 2 2 3 2 2 2 2 2 2 2 2 2 2 2		11 3
002Dh			
002Eh			
002Fh			<u> </u>

- X: Undefined
 NOTES:

 1. The blank regions are reserved. Do not access locations in these regions.
 2. The CSPROINI bit in the OFS register is set to 0.

 - 3. This register is not implemented in the R8C/2J Group.

SFR Information (2)⁽¹⁾ Table 4.2

0039th	Address	Register	Symbol	After reset
Voltage Detection Register 2(2)		i togicioi	- Symmet	7
0033h		Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0033h 0034h 0034h 0035h 0036h 0036	0032h		VCA2	00h ⁽³⁾
0033h 0036h 0036h 0036h 0036h 0037h 0038h 0037h 0038h 0038				
0038h Voltage Monitor 1 Circuit Control Register ⁽⁶⁾ WY1C 00001010b 0037h Voltage Monitor 2 Circuit Control Register ⁽⁶⁾ WV2C 00000010b 0038h Voltage Monitor 2 Circuit Control Register ⁽⁶⁾ WV2C 00000010b 0039h Voltage Monitor 0 Circuit External Input Control Register VCAB 00h 0039h Voltage Detection Circuit External Input Control Register VCAB 00h 0030h Voltage Detection Circuit External Input Control Register VCAC 00h 0030h Voltage Monitor Circuit External Input Control Register VCAC 00h 0039h Voltage Monitor Circuit External Input Control Register VCAC 00h 0039h Voltage Monitor Circuit External Input Control Register VCAC 00h 0040h Comparator 2 Interrupt Control Register VCMP1IC XXXXXX000b 0041h Comparator 2 Interrupt Control Register VCMP2IC XXXXXX000b 0041h Comparator 2 Interrupt Control Register TREIC XXXXXX000b 0041h Timer RE Interrupt Control Register SZRIC XXXXXX000b 0	0033h			
00038h				
0037h Voltage Monitor 2 Circuit Control Register(9) VW2C 00000010b 0038h Voltage Monitor 3 Circuit Control Register(9) VW6C 10000010b(9) 0038h Voltage Monitor Gircuit External Input Control Register VCAB 00h 0038h Voltage Detection Circuit External Input Control Register ALCMR 00h 00350h Comparator Mode Register ALCMR 00h 0036h Voltage Monitor Circuit External Input Control Register VCAC 00h 0037h Voltage Monitor Circuit External Input Control Register VCAC 00h 0049h VORPTIC XXXXXX000b VCMPTIC XXXXXX000b 0041h Comparator 1 Interrupt Control Register VCMPTIC XXXXXX000b XXXXXX000b 0043h Comparator 2 Interrupt Control Register VCMPTIC XXXXXX000b XXXXXX000b 0044h Comparator 2 Interrupt Control Register TREIC XXXXXX000b XXXXXX000b 0044h Timer RE Interrupt Control Register TREIC XXXXXX000b XXXXXX000b 0044h UART2 Transmit Interrupt Control Register SZTIC<				
O038h				
100X011b 40				
0039sh 0038h Votage Detection Circuit External Input Control Register VCAB 00h 0038bh Votage Detection Circuit External Input Control Register ALCMR 00h 0035ch Votage Monitor Circuit Edge Select Register VCAC 00h 0035ch Vodac 00h 00h 0035ch VCAC 00h 00h 0035ch VCAC 00h 00h 0035ch VCAC 00h 00h 004ch VCAC 00h 00h 004ch VCAC 00h 00h 004ch VCAC 00h 00h 004ch VCAC 00h 00h 004dh VCMP2IC XXXXXX000b XXXXXX000b 004dh VCMP2IC XXXXXX000b	0038h	Voltage Monitor 0 Circuit Control Register ⁽²⁾	VW0C	
003Ah Voltage Detection Circuit External Input Control Register VCAB 00h 003Ch Comparator Mode Register ALCMR 00h 003Ch Comparator Mode Register VCAC 00h 003Eh Voltage Monitor Circuit Edge Select Register VCAC 00h 003Eh Oute VCMP IC XXXXX000b 004Eh Comparator 1 Interrupt Control Register VCMP2IC XXXXX000b 0043h Comparator 2 Interrupt Control Register VCMP2IC XXXXX000b 0043h Oud4h VCMP2IC XXXXX000b 0045h Ou46h VCMP2IC XXXXX000b 0048h VCMP2IC XXXXX000b VCMP2IC XXXXX000b 0048h VCMP2IC XXXXX000b VCMP2IC XXXXX000b 0048h VCMP2IC XXXXX000b VCMP2IC XXXXX000b 0045h VCMP2IC XXXXX000b XXXXX000b XXXXX000b 0044h VCMP2IC XXXXX000b XXXXX000b XXXXX000b 0045h VCMP2IC XXXXX000b	00001			1100X011b ⁽⁴⁾
0038h Voltage Detection Circuit External Input Control Register VCAB 00h 003Ch Comparator Mode Register ALCMR 00h 003Dh Voltage Monitor Circuit Edge Select Register VCAC 00h 003Fh Voltage Monitor Circuit Edge Select Register VCAC 00h 004Dh Voltage Monitor Circuit Edge Select Register VCMP1C XXXXX000b 004Dh VCMP1C XXXXX000b VCMP2IC XXXXXX000b 0042h Comparator 1 Interrupt Control Register VCMP2IC XXXXXX000b VCMP2IC XXXXXX000b 0043h O044h Interrupt Control Register VCMP2IC XXXXXX000b VCMP2IC XXXXXX000b 0044h Interrupt Control Register ITREIC XXXXXX000b XXXXXX000b XXXXXX000b XXXXXX000b XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX				
003Ch Comparator Mode Register ALCMR 00h 003Ch Voltage Monitor Circuit Edge Select Register VCAC 00h 003Eh VOLAC 00h 003Eh VCAC 00h 004Dh VCMP2IC XXXXX000b 0041h Comparator 1 Interrupt Control Register VCMP2IC XXXXX000b 0043h O044h VCMP2IC XXXXX000b 0044h VCMP2IC XXXXX000b 0044h VCMP2IC XXXXX000b 0048h VCMP2IC XXXXX000b 0049h VCMP2IC XXXXX000b 0040h VCMP2IC XXXXX000b 0041h VCMP2IC CXXXXX000b XXXXX000b 0044h VCMP2IC CXXXXX000b XXXXX000b 0044h VCMP2IC CXXXXX000b XXXXX000b 0044h VCMP2IC CXXXXX000b		Voltago Dotaction Circuit External Input Control Pagistar	VCAR	00h
003Dh Voltage Monitor Circuit Edge Select Register VCAC 00h 003Eh 0040h 0040h 0040h 0040h 0040h 0041h Comparator 1 Interrupt Control Register VCMP1IC XXXXX000b 0042h Comparator 2 Interrupt Control Register VCMP2IC XXXXX000b 0043h 0044h 0046h 0046h 0047h 0048h 0049h 0047h 0048h 0049h TREIC XXXXX000b 0048h 0047h XXXXX000b XXXXX000b 0048h UART2 Transmit Interrupt Control Register(6) SZTIC XXXXX000b 0046h UART2 Receive Interrupt Control Register SZRIC XXXXX000b 0047h Key Input Interrupt Control Register KUPIC XXXXX000b 0046h UART0 Transmit Interrupt Control Register CMP1IC XXXXX000b 0047h UART0 Transmit Interrupt Control Register SOTIC XXXXX000b 0052h UART0 Transmit Interrupt Control Register SORIC XXXXX000b 0053h UART0 Transmit		Comparator Mode Register		* *
003Eh 003Fh 0040h Comparator 1 Interrupt Control Register VCMP1IC XXXXX000b 0041h 0047h 0048h Comparator 2 Interrupt Control Register VCMP2IC XXXXX000b 0043h 0046h WCMP2IC XXXXX000b 0047h 0046h WCMP2IC XXXXX000b 0047h 0048h WCMP2IC XXXXX000b 0049h 0049h TREIC XXXXX000b 0049h 0040h WART2 Transmit Interrupt Control Register(6) S2RIC XXXXX000b 004Ch 004Ch WART2 Receive Interrupt Control Register S2RIC XXXXX000b 004Eh 004Eh WIPIC XXXXX000b XXXXX000b 004Eh 005D WIPIC XXXXX000b XXXXX000b 004Eh 005D WARTO Receive Interrupt Control Register CMP1IC XXXXX000b 005Sh 005Sh UARTO Receive Interrupt Control Register S0RIC XXXXX000b 005Sh 005Sh Imer RB Interrupt Control Register TRBIC XXXXX000b 005Sh 005Sh Imer RE Interrupt Control Register INT Interrupt Control Register TRBIC XXXXX000b 005Sh 005Sh Imer RE Interrupt Control Register				
0040h Comparator 1 Interrupt Control Register VCMP1IC XXXXX000b 0042h Comparator 2 Interrupt Control Register VCMP2IC XXXXX000b 0043h 0044h 0046h 0047h 0046h 0047h 0048h 0048h 0048h 0048h 0049h 0048h 004Ah Timer RE Interrupt Control Register(**) \$271C XXXXX000b 004Bh UART2 Transmit Interrupt Control Register(**) \$271C XXXXX000b 004Ch UART2 Receive Interrupt Control Register(**) \$281C XXXXX000b 004Dh Key Input Interrupt Control Register \$281C XXXXX000b 004Eh 005th Compare 1 Interrupt Control Register \$271C XXXXX000b 005th LURT0 Transmit Interrupt Control Register \$281C XXXXX000b 005th LURT0 Transmit Interrupt Control Register \$30TC XXXXX000b 005sh LURT0 Transmit Interrupt Control Register \$30TC XXXXX000b 005sh UART0 Receive Interrupt Control Register \$30TC XXXXX000b 005sh				
0041h Comparator 1 Interrupt Control Register VCMP2IC XXXXX000b 0042h Comparator 2 Interrupt Control Register VCMP2IC XXXXX000b 0043h 0044h 0045h 0046h 0047h 0048h 0048h 0048h 004Ch 004Bh 004Ch 004Ch 004Ch 004Ch 004Eh 004Eh 004Eh 005D	003Fh			
0042h Comparator 2 Interrupt Control Register VCMP2IC XXXXX000b 0043h 0044h 0046h 0047h 0048h 0049h 0048h 0049h 0041h 0042h 0042h 0042h 0042h 0044h 0044h 0044h 0044h 0050h 0051				
0043h 0044h 0045h 0046h 0047h 0047h 0048h 0049h 0049h Timer RE Interrupt Control Register ⁽⁶⁾ SZTIC 0048h UART2 Transmit Interrupt Control Register ⁽⁶⁾ SZRIC 004D UART2 Receive Interrupt Control Register SZRIC 004D Key Input Interrupt Control Register KUPIC 004Eh VAXXXX000b 004Eh VAXXXX000b 004Eh VAXXXX000b 004Eh VAXXXX000b 0050h Compare 1 Interrupt Control Register CMP1IC 0051h UART0 Transmit Interrupt Control Register SORIC 0053h UART0 Receive Interrupt Control Register SORIC 0053h UART0 Receive Interrupt Control Register TRAIC 0055h Timer RA Interrupt Control Register TRAIC 0055h Timer RE Interrupt Control Register TRBIC 0058h Timer RE Interrupt Control Register TRFIC 0056h Timer RE Interrupt Control Register TRFIC 0055h Compar				
0044h 0045h 0046h 0047h 0048h 0049h 0049h 0049h 0049h 0049h 0049h 0049h 0048h 0058h 0058		Comparator 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0045h 0046h 0047h 0048h 0049h 0047h 0049h 0047h 0059h 0047h 0059h 0047h 0059h 0047h 0059h 0047h 0059h 0059				
0046h 0047h 0048h 0049h 0048h 0049h 0048h 0049h 0048h 0059h 0059				
0047h				
0049h 004Ah Timer RE Interrupt Control Register(6) TREIC XXXXX000b 004Ah UART2 Transmit Interrupt Control Register(6) S2TIC XXXXX000b 004Ch UART2 Receive Interrupt Control Register KUPIC XXXXX000b 004Bh Key Input Interrupt Control Register KUPIC XXXXX000b 004Fh Compare 1 Interrupt Control Register CMP1IC XXXXX000b 0050h Compare 1 Interrupt Control Register SOTIC XXXXX000b 0051h UARTO Transmit Interrupt Control Register SORIC XXXXX000b 0052h UARTO Receive Interrupt Control Register SORIC XXXXX000b 0053h OSSSh OSSSh OSSSh 0056h Timer RA Interrupt Control Register TRAIC XXXXX000b 0057h NT1 Interrupt Control Register INT1IC XXXXX000b 0058h Timer RF Interrupt Control Register INT1IC XXXXX000b 0058h Interrupt Control Register CMPOIC XXXXX000b 0059h INT0 Interrupt Control Register CAPIC XXXXX000b				
004Ah Timer RE Interrupt Control Register ⁽⁶⁾ TREIC XXXXX000b 004Bh UART2 Transmit Interrupt Control Register ⁽⁶⁾ S2TIC XXXXX000b 004Ch UART2 Receive Interrupt Control Register S2RIC XXXXX000b 004Bh Key Input Interrupt Control Register KUPIC XXXXX000b 004Eh 004Fh Compare 1 Interrupt Control Register CMP1IC XXXXX000b 005bh Compare 1 Interrupt Control Register SORIC XXXXX000b 0051h UART0 Transmit Interrupt Control Register SORIC XXXXX000b 0052h UART0 Receive Interrupt Control Register SORIC XXXXX000b 0053h OSSA Compare 1 Interrupt Control Register TRAIC XXXXX000b 0055h Timer Receive Interrupt Control Register TRAIC XXXXX000b 0055h Timer RA Interrupt Control Register TRAIC XXXXX000b 0055h Timer RB Interrupt Control Register TRBIC XXXXX000b 0058h Timer RF Interrupt Control Register TRFIC XXXXX000b 005Ch Compare 0 Interrupt Control	0048h			
004Bh UART2 Transmit Interrupt Control Register(6) SZTIC XXXXX000b 004Ch UART2 Receive Interrupt Control Register(6) SZRIC XXXXX000b 004Bh Key Input Interrupt Control Register KUPIC XXXXX000b 004Eh Compare 1 Interrupt Control Register CMP1IC XXXXX000b 0050h Compare 1 Interrupt Control Register SOTIC XXXXX000b 0051h UART0 Transmit Interrupt Control Register SORIC XXXXX000b 0052h UART0 Receive Interrupt Control Register SORIC XXXXX000b 0053h Imperation of the Control Register TRAIC XXXXX000b 0054h Imperation of the Control Register TRAIC XXXXX000b 0057h Imperation of the Control Register Invalid Control Register Invalid Control Register 0058h Timer RF Interrupt Control Register TREIC XXXXX000b 0059h Invalid Control Register Invalid Control Register Invalid Control Register 0059h Invalid Control Register Invalid Control Register Invalid Control Register Invalid Control Register Invali	0049h			
004Ch UART2 Receive Interrupt Control Register S2RIC XXXXX000b 004Dh Key Input Interrupt Control Register KUPIC XXXXX000b 004Eh WIPIC XXXXX000b 004Fh WIPIC XXXXX000b 0050h Compare 1 Interrupt Control Register CMP1IC XXXXX000b 0051h UART0 Receive Interrupt Control Register S0RIC XXXXX000b 0053h WART0 Receive Interrupt Control Register S0RIC XXXXX000b 0053h WART0 Receive Interrupt Control Register TRAIC XXXXX000b 0055h Timer RA Interrupt Control Register TRBIC XXXXX000b 0057h WARX000b WARX000b WARX000b 0058h Timer RB Interrupt Control Register TRFIC XXXXX000b 0058h Timer RF Interrupt Control Register TRFIC XXXXX000b 005Ah INT0 Interrupt Control Register CMP0IC XXXXX000b 005Ch Compare O Interrupt Control Register CAPIC XXXXX000b 005Ch WARX000b WARX000b WARX000b		Timer RE Interrupt Control Register ⁽⁶⁾		
0040h Key Input Interrupt Control Register KUPIC XXXXX000b 004Eh 004Fh Compare 1 Interrupt Control Register CMP1IC XXXXX000b 0050h Compare 1 Interrupt Control Register SORIC XXXXX000b 0051h UARTO Transmit Interrupt Control Register SORIC XXXXX000b 0053h UARTO Receive Interrupt Control Register SORIC XXXXX000b 0053h INTERRA Interrupt Control Register TRAIC XXXXX000b 0055h Timer RB Interrupt Control Register TRBIC XXXXX000b 0059h INT1 Interrupt Control Register INT1IC XX00X000b 0059h Timer RF Interrupt Control Register TRFIC XXXXX000b 005Ch Compare 0 Interrupt Control Register CMP0IC XXXXX000b 005Ch Compare 0 Interrupt Control Register INT0IC XX00X000b 005Fh Capture Interrupt Control Register CAPIC XXXXX000b 006Ch 006Ch 006Ch 006Ch 006Ch 006Sh 006Gh 006Ch 006Ch 006Ch				
004Eh 004Fh 004Fh 0050h Compare 1 Interrupt Control Register CMP1IC XXXXX000b 0051h UART0 Transmit Interrupt Control Register S0TIC XXXXX000b 0052h UART0 Receive Interrupt Control Register S0RIC XXXXX000b 0053h 0054h 0054h 0054h 0055h Timer RA Interrupt Control Register TRAIC XXXXX000b 0057h 0058h Timer RB Interrupt Control Register TRBIC XXXXX000b 0059h INT1 Interrupt Control Register INT1IC XX00X000b 005Ah INT0IC XXXXX000b 005Ch Compare 0 Interrupt Control Register TRFIC XXXXX000b 005Dh INT0I Interrupt Control Register INT0IC XXXXX000b 005Eh Capture Interrupt Control Register CAPIC XXXXX000b 005Eh 0060h 0060h 0060h 0063h 0064h 0066h 0066h 0066h 0066h 0066h 0066h 0068h 0068h 0068h				
004Fh 0050h Compare 1 Interrupt Control Register CMP1IC XXXXX000b 0051h UART0 Transmit Interrupt Control Register S0TIC XXXXX000b 0052h UART0 Receive Interrupt Control Register S0RIC XXXXX000b 0053h 0054h 0055h 0056h 0055h 1 0056h 1 0057h 0058h 1 0058h 1 0058h 1 1 1 0 0 0059h 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		Key Input Interrupt Control Register	KUPIC	XXXXX000b
0050h Compare 1 Interrupt Control Register CMP1IC XXXXX000b 0051h UARTO Transmit Interrupt Control Register SOTIC XXXXX000b 0052h UARTO Receive Interrupt Control Register SORIC XXXXX000b 0053h Warron Receive Interrupt Control Register TRAIC XXXXX000b 0055h Warron Receive Interrupt Control Register TRAIC XXXXX000b 0057h Warron Receive Interrupt Control Register Interrupt Control Register Interrupt Control Register 0058h Timer RB Interrupt Control Register Interrupt Control Register Interrupt Control Register 005Ah Warron Register CMPOIC XXXXX000b 005Dh Introl Interrupt Control Register Introl XXXXX000b 005Eh Warron Register Introl XXXXX000b 0				
0051h UARTO Transmit Interrupt Control Register SOTIC XXXXX000b 0052h UARTO Receive Interrupt Control Register SORIC XXXXX000b 0053h 0054h 0055h 0057h 0058h Timer RA Interrupt Control Register TRBIC XXXXX000b 0059h INT1 Interrupt Control Register INT1IC XX00X000b 0059h INT1 Interrupt Control Register TRFIC XXXXX000b 005Ch Compare 0 Interrupt Control Register CMP0IC XXXXX000b 005Eh INT0 Interrupt Control Register INT0IC XX00X000b 005Eh 005Eh 005Fh Capture Interrupt Control Register CAPIC XXXXX000b 006h 006h 006h 006h		Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0052h UART0 Receive Interrupt Control Register SORIC XXXXX000b 0053h 0054h 0055h 0056h 0066h 0066h 0067h 0068h 0068h 0068h 0068h 0068h 0068h 0066h 0068h		UARTO Transmit Interrupt Control Register		
0053h 0054h 0055h				
0055h 0056h Timer RA Interrupt Control Register TRAIC XXXXX000b 0057h	0053h	·		
0056h Timer RA Interrupt Control Register TRAIC XXXXX000b 0057h				
0057h 0058h Timer RB Interrupt Control Register TRBIC XXXXX000b 0059h INT1 Interrupt Control Register INT1IC XX00X000b 005Ah 005Bh Timer RF Interrupt Control Register TRFIC XXXXX000b 005Ch Compare 0 Interrupt Control Register CMP0IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Eh 005Fh Capture Interrupt Control Register CAPIC XXXXX000b 0060h 0061h 0062h 0063h 0064h 0065h 0066h 0067h 0068h 0069h 0069h 0060Ah 0060Ah 0069h 0069h				
0058h Timer RB Interrupt Control Register TRBIC XXXXX000b 0059h INT1 Interrupt Control Register INT1IC XX00X000b 005Ah Image: Control Register TRFIC XXXXX000b 005Ch Compare 0 Interrupt Control Register CMP0IC XXXXX000b 005Ch INT0 Interrupt Control Register INT0IC XX00X000b 005Eh Copture Interrupt Control Register CAPIC XXXXX000b 0060h 0061h 0062h 0063h 0063h 0064h 0065h 0066h 0066h 0067h 0068h 0069h 0069h 0060A 0060A 0060A		Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0059h INT1 Interrupt Control Register INT1IC XX00X000b 005Ah 005Bh Timer RF Interrupt Control Register TRFIC XXXXX000b 005Ch Compare 0 Interrupt Control Register CMP0IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Eh Capture Interrupt Control Register CAPIC XXXXX000b 0060h 0061h 0062h 0063h 0064h 0065h 0066h 0067h 0068h 0067h 0068h 0069h 0069h 006Ah 006Ah 006Ah		Timor BB Interrupt Control Bogister	TRRIC	VVVVV000h
005Ah 005Bh Timer RF Interrupt Control Register TRFIC XXXXX000b 005Ch Compare 0 Interrupt Control Register CMP0IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Fh Capture Interrupt Control Register CAPIC XXXXX000b 0060h 0061h 0062h 0063h 0063h 0064h 0065h 0066h 0066h 0067h 0068h 0069h 0069h 0060h 0060h 0060h		INT1 Interrupt Control Register		
005Bh Timer RF Interrupt Control Register TRFIC XXXXX000b 005Ch Compare 0 Interrupt Control Register CMP0IC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Eh Capture Interrupt Control Register CAPIC XXXXX000b 0060h 0061h 0062h 0063h 0064h 0065h 0066h 0067h 0068h 0068h 0069h 0069h 0069h 0060Ah 0060Ah		THE THOUSE CONTROL TO GISTON		70.007.0002
005Ch Compare 0 Interrupt Control Register CMPOIC XXXXX000b 005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Eh Capture Interrupt Control Register CAPIC XXXXX000b 0060h 0061h 0062h 0063h 0064h 0065h 0066h 0067h 0068h 0068h 0069h 0060h 0069h 006Ah 006Ah	005Bh			XXXXX000b
005Eh Capture Interrupt Control Register CAPIC XXXXX000b 0060h 0061h 0062h 0062h 0063h 0064h 0065h 0065h 0066h 0067h 0068h 0068h 0069h 0069h 0068h 0069h 0068h 0068h 0068h 0069h 0068h				
005Fh Capture Interrupt Control Register CAPIC XXXXX000b 0060h 0061h 0062h 0062h 0062h 0063h 0064h 0064h 0065h 0066h 0066h 0067h 0068h 0068h 0069h 0069h 0069h 0068h 0068h 0069h 0068h 0068h 0068h 0069h 0068h		INT0 Interrupt Control Register	INT0IC	XX00X000b
0060h 0061h 0062h 0063h 0064h 0065h 0066h 0067h 0068h 0069h 006Ah			0.50	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
0061h 0062h 0063h 0064h 0065h 0066h 0067h 0068h 0069h 006Ah		Capture Interrupt Control Register	CAPIC	XXXXXUUUb
0062h 0063h 0064h 0065h 0066h 0067h 0068h 0069h 006Ah				
0063h 0064h 0065h 0066h 0067h 0068h 0069h 006Ah				
0064h 0065h 0066h 0067h 0068h 0069h 006Ah				
0066h 0067h 0068h 0069h 006Ah				
0067h 0068h 0069h 006Ah				
0068h 0069h 006Ah				
0069h 006Ah				
006Ah				
UUDDI I	006An			
006Ch				
006Dh				
006Eh				
006Fh				

X: Undefined

- The blank regions are reserved. Do not access locations in these regions.
- Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register. The LVD0ON bit in the OFS register is set to 1 and hardware reset. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3. This register is not implemented in the R8C/2J Group.

SFR Information (3)⁽¹⁾ Table 4.3

Address	Register	Symbol	After reset
0070h	· · · · · · · · · · · · · · · · · · ·		
0071h			
0071h			
0072h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			
0080h			
0080h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Bh			
009Dh			
009Eh			
009Fh			
	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h	j		XXh
00A8h			
00A9h			
00A9II			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			

Table 4.4 SFR Information (4)⁽¹⁾

Address	Register	Symbol	After reset
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			
00C0h			
00C1h			
00C2h			
00C3h 00C4h			
00C4h			
00C5fi			
00C6H			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh 00DEh			
00DEh 00DFh			
00E0h			
00E0H	Port P1 Register	P1	00h
00E1h			55.7
00E3h	Port P1 Direction Register	PD1	00h
00E4h		-	
00E5h	Port P3 Register	P3	00h
00E6h	V ***		
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	00h
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	00h
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
V: Undofined			

SFR Information (5)⁽¹⁾ Table 4.5

Address	Register	Symbol	After reset
00F0h	regional	Cymbol	71101 10001
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h	Pin Select Register 2	PINSR2	00h
00F7h	Till Select (register 2	TINONZ	0011
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00F9h	INT Input Filter Select Register	INTF	
00FAn	Key Input Enable Register	KIEN	00h 00h
	Rey Input Enable Register		
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh			
00FFh			
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh	Time No Filmary Register	TRUTT	1111
0110h			
0110h			
0111h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register ⁽²⁾	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register ⁽²⁾	TREMIN	00h
011Ah	Timer RE Hour Data Register ⁽²⁾	TREHR	00h
011Bh	Timer RE Day of Week Data Register ⁽²⁾	TREWK	00h
011Ch	Timer RE Control Register 1 ⁽²⁾	TRECR1	00h
011Dh	Timer RE Control Register 12(2)	TRECR2	00h
	Timer RE Control Register 2(2)	-	
011Eh	Timer RE Clock Source Select Register (2)	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0124h 0125h			
0124h			
0124h 0125h 0126h 0127h			
0124h 0125h 0126h			
0124h 0125h 0126h 0127h			
0124h 0125h 0126h 0127h 0128h			
0124h 0125h 0126h 0127h 0128h 0129h 012Ah			
0124h 0125h 0126h 0127h 0128h 0129h 012Ah 012Bh			
0124h 0125h 0126h 0127h 0128h 0129h 012Ah 012Bh 012Ch			
0124h 0125h 0126h 0127h 0128h 0129h 0129h 012Ah 012Bh 012Ch 012Dh			
0124h 0125h 0126h 0127h 0128h 0129h 012Ah 012Bh 012Ch			

- X: Undefined NOTE:

 1. The blank regions are reserved. Do not access locations in these regions
 - 2. This register is not implemented in the R8C/2J Group.

SFR Information (6)⁽¹⁾ Table 4.6

Address	Register	Symbol	After reset
0130h	•	,	
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh 013Eh			
013En			
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h 0149h			
0149h 014Ah			
014An			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h 0154h			
0154n			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh 015Fh			
0160h	UART2 Transmit/Receive Mode Register ⁽²⁾	U2MR	00h
0161h	UART2 Bit Rate Register ⁽²⁾	U2BRG	XXh
0162h	UART2 Transmit Buffer Register ⁽²⁾	U2TB	XXh
0163h	Ourt 2 Handriit Dullet Negloter /	02.0	XXh
0164h	UART2 Transmit/Receive Control Register 0 ⁽²⁾	U2C0	00001000b
0165h	UART2 Transmit/Receive Control Register 1(2)	U2C1	00000010b
0166h	UART2 Receive Buffer Register ⁽²⁾	U2RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh 016Fh			
UIOFII			

- X: Undefined
 NOTE:

 1. The blank regions are reserved. Do not access locations in these regions.
 2. This register is not implemented in the R8C/2J Group.

SFR Information (7)⁽¹⁾ Table 4.7

Address	Register	Symbol	After reset
	Register	Symbol	Alter reset
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Ch			
019Dh 019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h		<u> </u>	
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01/1111			l

SFR Information (8)⁽¹⁾ Table 4.8

٠	Dogister .	Cymala al	After
Address	Register	Symbol	After reset
01B0h			
01B1h			
01B2h		EMD 4	04000000
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h		EMD4	40000001//
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h	-		
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D0h			
01D8h			
01D8h			
01D9h 01DAh			
01DAn			
01000			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h		<u> </u>	
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
O I E I II			l

SFR Information (9)⁽¹⁾ Table 4.9

A -1 -1 1	Desirter	O:bI	A #
Address	Register	Symbol	After reset
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
017711			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020En			
020FII			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
021FII 0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
VEELII			l

Table 4.10 SFR Information (10)⁽¹⁾

Address	Register	Symbol	After reset
0230h	-	•	
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			
0240h			
0241h			
0241h			
0242H			
0243H 0244h			
024411 0245h			
0245f1 0246h			
0246h 0247h			
0247fi 0248h			
02480			
0249h			
024Ah			
024Bh			
024Ch			
024Dh			
024Eh			
024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h			
0261h			
0262h			
0263h			
0264h			
0265h			
0266h			
0267h			
0268h			
0269h			
026Ah			
026Bh			
026Ch			
026Dh			
026Eh 026Fh			
			l

SFR Information (11)⁽¹⁾ **Table 4.11**

O27th	Address	Register	Symbol	After reset
0271h		register	Cymbol	Alter reset
0272h	0270h			
0273h				
0274h				
0275h	0273h			
0276h 0278h 0288h 0288				
0277h	0276h			
0278h 027Ah 027Ah 027Ah 027Bh 027Ah 027Bh 027Ch 027Dh 027Eh 028Dh 028Dh 028Bh 028B	0277h			
0279h	0277h			
0278h				
0278h				
027Ch	0277th			
027Dh	027Ch			
027Fh 0280h	027Dh			
022Fh	027Fh			
0280h				
0281h				
0282h	0281h			
0283h	0287h			
0284h	0283h			
0285h	0284h			
0286h				
0287h 0288h 0299h 0299	0286h			
0288h 028Ah 028Bh 028Bh 028Ch 029Ch 029C	0287h			
0289h 028Ch 028Ch 028Eh 028Eh 028Eh 028Eh 028Eh 028Eh 028Eh 028Eh 028Eh 0290h 0290h 0290h 0291h 0292h 0293h 0293h 0293h 0293h 0299h 0298h 0299h 0299h 0299h 0299h 0299h 0299h 0299h 0298h 0299h 0299				
028Ah 028Bh 028Ch 028Bh 028Ch 028Bh 028Bh 028Bh 028Bh 028Bh 029Bh 0299h 0292h 0292	0289h			
028Bh 028Ch 028Bh 028Eh 028Eh 028Eh 028Eh 0290h 0290h 0291h 0292h 0293h 0293	028Ah			
028Ch 028Bh 028Fh 0299h 0299				
028Dh 028Eh 0290h Timer RF Register TRF 00h 0291h 00h 00h 00h 0291h 00h 00h 00h 0293h 0294h 00h 0295h 0296h 0296h 00h 0297h 00h 0299h Timer RF Control Register 2(4) TRFCR2 00h 0299h Timer RF Control Register 0 TRFCR0 00h 029Bh Timer RF Control Register 1 TRFM0 0000h(2) 029Ch Capture and Compare 0 Register TRFM0 0000h(2) 029Fh Compare 1 Register TRFM1 FFh 02A0h 02A1h 02A2h 02A3h 02A3h 02A3h 02A3h 02A3h 02A6h 02A7h 02A8h 02A8h 02AAh 02AAh 02AAh 02AAh 02ABh 02ACh 02ACh 02ACh	028Ch			
028Fh 0297h 0291h 0291h 0292h 0293h 0293h 0294h 0293h 0293h 0294h 0293h 02995h 02995h 02997h 02998h 02988h 029888h 029888h 029888h 029888h 029888h 029888h 029888h 02988h	028Dh			
0.28Fh	028Fh			
O291h	028Fh			
0291h	0290h	Timer RF Register	TRF	00h
0292h 0293h 0294h 0295h 0296h 0297h 0298h 0299h 0299h Timer RF Control Register 2(4) TRFCR2 029Ah Timer RF Control Register 0 TRFCR0 00h 029Bh Timer RF Control Register 1 TRFCR1 00h 029Ch Capture and Compare 0 Register TRFM0 0000h(2) 029Dh Compare 1 Register TRFM1 FFh 029Fh 02A0h FFFFh(3) FFFh 02A0h 02A1h FFFh FFFh 02A3h 02A4h 02A4h 02A5h 02A6h 02A7h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02ABh 02ABh 02ABh 02ABh 02ABh 02ABh 02ABh 02ABh 02ABh 02ABh 02ABh 02ABh	0291h	I Troughold		
0293h 0294h 0295h 0296h 0297h 0298h 0299h Timer RF Control Register 2 ⁽⁴⁾ TRFCR2 00h 0294h Timer RF Control Register 0 TRFCR0 00h 029Bh Timer RF Control Register 1 TRFCR1 00h 029Ch Capture and Compare 0 Register TRFM0 0000h(2) 029Fh FFFFh(3) FFFFh(3) 029Fh Compare 1 Register TRFM1 FFh 02A0h D2A1h FFFPh 02A2h 02A3h 02A3h 02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02A8h 02A9h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h	0292h			
0294h 0295h 0297h 0298h 0299h Timer RF Control Register 2(4) TRFCR2 00h 0299h Timer RF Control Register 0 TRFCR0 00h 029Bh Timer RF Control Register 1 TRFCR1 00h 029Ch Capture and Compare 0 Register TRFM0 0000h(2) 029Dh FFFFh(3) 029Eh Compare 1 Register TRFM1 FFh 029Fh 02A0h FFFh FFh 02A1h 02A2h FFFh FFh 02A3h 02A4h FF FF 02A6h 02A7h FF FF 02A9h 02A9h FF FF 02A9h FF FF FF 02A8h FF FF FF 02A8h FF FF FF 02A8h FF FF FF 02ABh FF FF FF 02ABh FF FF FF 02ABh <td< td=""><td>0293h</td><td></td><td></td><td></td></td<>	0293h			
0295h 0297h 0298h				
0297h 0298h 0299h Timer RF Control Register 2 ⁽⁴⁾ TRFCR2 00h 029Ah Timer RF Control Register 0 TRFCR0 00h 029Bh Timer RF Control Register 1 TRFCR1 00h 029Ch Capture and Compare 0 Register TRFM0 0000h(2) 029Dh FFFFh(3) FFFh 029Fh Compare 1 Register TRFM1 FFh 02A0h FFFh FFh 02A1h FFFh FFh 02A2h FFFh FFFh 02A3h FFFh FFFh 02A6h FFFA FFFh 02A8h FFFA FFFA 02ABh FFFA FFFA	0295h			
0297h	0296h			
0298h Timer RF Control Register 2 ⁽⁴⁾ TRFCR2 00h 029Ah Timer RF Control Register 0 TRFCR0 00h 029Bh Timer RF Control Register 1 TRFCR1 00h 029Ch Capture and Compare 0 Register TRFM0 0000h ⁽²⁾ 029Dh Compare 1 Register TRFM1 FFh 029Fh Compare 1 Register TRFM1 FFh 02A0h 02A1h 02A2h 02A3h 02A3h 02A4h 02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02AAh 02A9h 02AAh 02AAh 02AAh 02ABh 02ACh 02ACh 02ACh	0297h			
0299h Timer RF Control Register 2 ⁽⁴⁾ TRFCR2 00h 029Ah Timer RF Control Register 0 TRFCR0 00h 029Bh Timer RF Control Register 1 TRFCR1 00h 029Ch Capture and Compare 0 Register TRFM0 0000h(2) 029Dh Compare 1 Register TRFM1 FFh 029Fh 02A0h	0298h			
029Bh Timer RF Control Register 1 TRFCR1 00h 029Ch Capture and Compare 0 Register TRFM0 0000h(²) 029Bh Compare 1 Register TRFM1 FFh 029Fh TRFM1 FFh 02A0h FFFh FFh 02A1h Compare 1 Register FFh 02A0h FFFh FFh 02A1h FFH FFh 02A2h Compare 1 Register Compare 1 Register 02A1h FFFH FFh 02A2h Compare 1 Register Compare 1 Register 02A3h Compare 1 Register FFFH FFFH FFh FFH 02A3h Compare 1 Register Compare 1 Register 02A3h Compare 1 Register Compare 1 Register 02A4h Compare 1 Register Compare 1 Register 02A5h Compare 1 Register Compare 1 Register 02A6h Compare 1 Register Compare 1 Register FFh 02A5h Compare 1 Register Compare 1 Register FFh	0299h	Timer RF Control Register 2(4)	TRFCR2	00h
029Bh Timer RF Control Register 1 TRFCR1 00h 029Ch Capture and Compare 0 Register TRFM0 0000h(²) 029Bh Compare 1 Register TRFM1 FFh 029Fh TRFM1 FFh 02A0h FFFh FFh 02A1h Compare 1 Register FFh 02A0h FFFh FFh 02A1h FFH FFh 02A2h Compare 1 Register Compare 1 Register 02A1h FFFH FFh 02A2h Compare 1 Register Compare 1 Register 02A3h Compare 1 Register FFFH FFFH FFh FFH 02A3h Compare 1 Register Compare 1 Register 02A3h Compare 1 Register Compare 1 Register 02A4h Compare 1 Register Compare 1 Register 02A5h Compare 1 Register Compare 1 Register 02A6h Compare 1 Register Compare 1 Register FFh 02A5h Compare 1 Register Compare 1 Register FFh	0200H	Timer RF Control Register 0		
029Dh	0207th	Timer RF Control Register 1	TRFCR1	
029Dh	029Ch	Capture and Compare 0 Register	TRFM0	0000h(2)
029Eh Compare 1 Register TRFM1 FFh 029Fh 02A0h FFh 02A0h 02A1h FFh 02A2h 02A3h FFh 02A3h 02A4h FFh 02A4h FFH FFH 02A3h FFH FFH 02A4h FFH FFH 02A4h FFH FFH 02A5h FFH FFH 02A6h FFH FFH 02A8h FFH FFH 02A9h FFH FFH 02ABh FFH FFH 02ACh FFH FFH FFH FFH FFH		Captaro and Compare o Neglotor	1131 1010	
029Fh FFh 02A0h 02A1h 02A2h 02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02ABh 02ACh	029DH	Compare 1 Pegister	TDEM1	rrrrii~
02A0h 02A1h 02A2h 02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02AAh 02ABh 02ACh	029EII	Compare i Negistei	INFIVII	CCP
02A1h 02A2h 02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02A8h 02ACh	029711			ГГІІ
02A2h 02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02AAh 02ABh 02ACh				
02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02AAh 02ABh 02ABh				
02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02AAh 02ABh 02ABh				
02A5h 02A6h 02A7h 02A8h 02A9h 02A9h 02AAh 02ABh 02ACh				
02A6h 02A7h 02A8h 02A9h 02AAh 02AAh 02ABh 02ACh				
02A7h 02A8h 02A9h 02AAh 02AAh 02ABh 02ACh				
02A8h 02A9h 02AAh 02ABh 02ACh				
02A9h 02AAh 02ABh 02ACh				
02AAh 02ABh 02ACh				
02ABh 02ACh				
02ACh				
02AEh				
02AFh	U∠AFN			

X: Undefined

- NOTES:

 1. The blank regions are reserved. Do not access locations in these regions.
 2. After input capture mode.
 3. After output compare mode.
 4. This register is not implemented in the R8C/2J Group.

SFR Information (12)⁽¹⁾ **Table 4.12**

Address	Register	Symbol	After reset
02B0h 02B1h			
02B1h 02B2h			
02B2h			
02B3h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			
02C0h			
02C1h			
02C2h			
02C3h			
02C4h			
02C5h 02C6h			
02C6h 02C7h			
02C7fi 02C8h			
02C8fi 02C9h			
02C3h			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh 02DCh			
02DCh 02DDh			
02DEh			
02DFh			
02E0h			
022011	1	1	l
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh	Pin Select Register 4	PINSR4	00h
02FCh			
02FDh			
02FEh	LTimes DE Outset Control Desister	TDEOUT	004
02FFh	Timer RF Output Control Register	TRFOUT	00h
	Ontion Function Colort Register	LOFE	(Note 2)
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

- NOTES:

 1. The blank regions are reserved. Do not access locations in these regions.

 2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

5.1 R8C/2H Group

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc	Supply voltage		-0.3 to 6.5	V
Vı	Input voltage		-0.3 to Vcc + 0.3	V
Vo	Output voltage		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	Topr = 25°C	500	mW
Topr	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
Tstg	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Param	otor	Conditions		Standard		Unit
Symbol	Farameter		Conditions	Min.	Тур.	Max.	Unit
Vcc	Supply voltage			2.2	-	5.5	V
Vss	Supply voltage			-	0	-	V
ViH	Input "H" voltage			0.8 Vcc	-	Vcc	V
VIL	Input "L" voltage			0	_	0.2 Vcc	V
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)		-	-	-160	mA
IOH(sum)	Average sum output "H" current	Sum of all pins IOH(avg)		-	=	-80	mA
IOH(peak)	Peak output "H" current	All pins		_	-	-10	mA
IOH(avg)	Average output "H" current	All pins		-	-	-5	mA
IOL(sum)	Peak sum output "L" currents	Sum of all pins IOL(peak)		-	=	160	mA
IOL(sum)	Average sum output "L" currents	Sum of all pins IOL(avg)		-	=	80	mA
IOL(peak)	Peak output "L" currents	All pins		-	-	10	mΑ
IOL(avg)	Average output "L" current	All pins		_	-	5	mA
f(XCIN)	XCIN clock input oscillation	frequency	2.2 V ≤ Vcc ≤ 5.5 V	0	-	70	kHz
=	System clock	OCD2 = 0 XCIN clock selected	2.2 V ≤ Vcc ≤ 5.5 V	0	=	70	kHz
		OCD2 = 1 On-chip oscillator clock selected	HRA01 = 0 Low-speed on-chip oscillator selected	=	125	=	kHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.7 V ≤ Vcc ≤ 5.5 V	_	=	8	MHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.2 V ≤ Vcc ≤ 5.5 V	=	_	4	MHz

- 1. Vcc = 2.2 to 5.5 V at $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. The typical values when average output current is 100 ms.

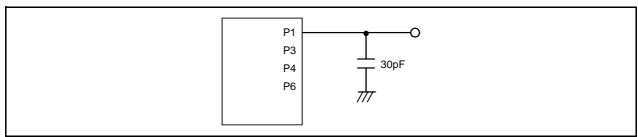


Figure 5.1 Ports P1, P3, P4, and P6 Timing Measurement Circuit

Table 5.3 Flash Memory (Program ROM) Electrical Chara

Cumbal	Parameter	Conditions		Unit		
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Uniit
=	Program/erase endurance ⁽²⁾		100 ⁽³⁾	=	=	times
_	Byte program time		-	50	400	μS
_	Block erase time		-	0.4	9	S
td(SR-SUS)	Time delay from suspend request until suspend		-	_	97 + CPU clock × 6 cycles	μS
_	Interval from erase start/restart until following suspend request		650	_	_	μS
_	Interval from program start/restart until following suspend request		0	_	_	ns
=	Time from suspend until program/erase restart		=	-	3 + CPU clock × 4 cycles	μS
_	Program, erase voltage		2.7	-	5.5	V
-	Read voltage		2.2	-	5.5	V
=	Program, erase temperature		0	=	60	°C
=	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	_	-	year

- NOTES:

 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60°C, unless otherwise specified.
 - 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

- However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

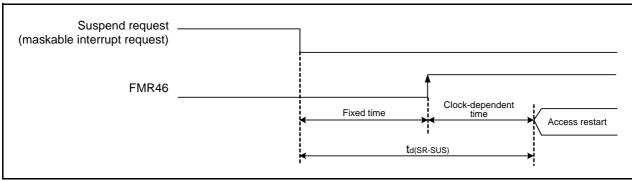


Figure 5.2 Time delay until Suspend

Table 5.4 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
	Falameter	Condition	Min.	Тур.	Max.	Unit
Vdet0	Voltage detection level		2.2	2.3	2.4	V
=	Voltage detection circuit self power consumption VCA25 = 1, Vcc = 5.0 V		=	0.9	=	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		=	=	300	μ\$
Vccmin	MCU operating voltage minimum value		2.2	-	-	V

NOTES:

- 1. The measurement condition is Vcc = 2.2 V to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version).
- 2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.5 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
	Farameter	Condition	Min.	Тур.	Max.	Ullit
Vdet1	Voltage detection level ⁽⁴⁾		2.70	2.85	3.00	V
_	Voltage monitor 1 interrupt request generation time ⁽²⁾		_	40	_	μS
=	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	=	0.6	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		-	_	100	μS

NOTES:

- 1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
- 4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.6 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet2	Voltage detection level		3.3	3.6	3.9	V
_	Voltage monitor 2 interrupt request generation time ⁽²⁾		_	40	-	μS
_	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	-	0.6	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		=	=	100	μS

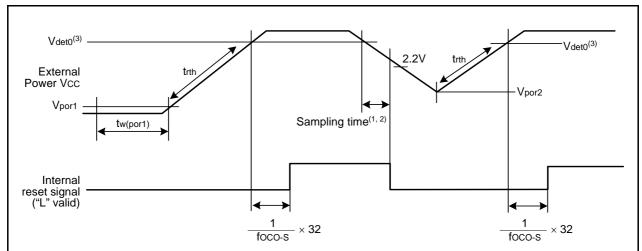
- 1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
- 3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.7 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition		Unit		
	Falametei	Condition	Min.	Тур.	Max.	Offic
Vpor1	Power-on reset valid voltage ⁽⁴⁾		-	-	0.1	V
Vpor2	Power-on reset or voltage monitor 0 reset valid voltage		0	_	Vdet0	V
trth	External power Vcc rise gradient(2)		20	_	_	mV/msec

NOTES:

- 1. The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. This condition (external power Vcc rise gradient) does not apply if Vcc ≥ 1.0 V.
- 3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
- 4. tw(por1) indicates the duration the external power Vcc must be held below the effective voltage (Vpor1) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30 s or more if -20°C ≤ Topr ≤ 85°C, maintain tw(por1) for 3,000 s or more if -40°C ≤ Topr < -20°C.</p>



- 1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
- 2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
- 3. Vdeto indicates the voltage detection level of the voltage detection 0 circuit. Refer to 6. Voltage Detection Circuit for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.8 Comparator Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vref	Internal reference voltage	$VCC = 5.0 \pm 5.0 \text{ V}, \text{ Topr} = 25^{\circ}\text{C}$	TBD	1.25	TBD	V
			TBD	1.25	TBD	V
CVREF	External reference voltage input range		-	TBD	TBD	V
VCMP1, VCMP2	External comparison voltage input range		-	TBD	TBD	V
=	Offset		=	TBD	TBD	mV
=	Response time		=	TBD	TBD	μS
_	Comparator self power consumption		-	TBD	TBD	μΑ

NOTE:

Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
fOCO-F	High-speed on-chip oscillator frequency temperature • supply voltage dependence	Vcc = 4.75 V to 5.25 V 0° C \leq Topr \leq 60°C ⁽²⁾	7.76	8	8.24	MHz
		Vcc = 2.7 V to 5.5 V -20° C \leq Topr \leq 85 $^{\circ}$ C ⁽²⁾	7.68	8	8.32	MHz
		Vcc = 2.7 V to 5.5 V -40°C \leq Topr \leq 85°C(2)	7.44	8	8.32	MHz
		Vcc = 2.2 V to 5.5 V -20° C \leq Topr \leq 85 $^{\circ}$ C ⁽²⁾	TBD	8	TBD	MHz
		Vcc = 2.2 V to 5.5 V -40°C \leq Topr \leq 85°C(2)	TBD	8	TBD	MHz

NOTES:

- 1. The measurement condition is $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.
- 2. These standard values show when the HRA1 register is set to the value before shipment and the HRA2 register is set to 00h.

Table 5.10 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Svmbol	Parameter	Condition		Unit		
Symbol	r alametei	Condition	Min.	Тур.	Max.	Offic
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
_	Oscillation stability time		-	10	100	μS
_	Self power consumption at oscillation	$VCC = 5.0 \text{ V}, \text{ Topr} = 25^{\circ}\text{C}$	_	15	1	μА

NOTE:

1. Vcc = 2.2 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.11 Power Supply Circuit Timing Characteristics

Svmbol	Parameter	Condition	Standard			Unit
Symbol	Falanetei	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	=	TBD	μS
td(R-S)	STOP exit time ⁽³⁾		-	-	TBD	μS

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = 25°C.
- 2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
- 3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

^{1.} The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition	S	Unit		
Symbol			Condition	Min.	Тур.	Max.	Offic
Vон	Output "H" voltage		Iон = −5 mA	Vcc - 2.0	-	Vcc	V
			IOH = -200 μA	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage		IoL = 5 mA	-	-	2.0	V
			IoL = 200 μA	-	-	0.45	V
VT+-VT-	Hysteresis	INT0, INT1, KI0, KI1, KI2, KI3, RXD0, RXD2, CLK0, CLK2		0.1	0.5	_	V
		RESET		0.1	1.0	_	V
Іін	Input "H" current		VI = 5 V, Vcc = 5 V	_	_	5.0	μΑ
lı∟	Input "L" current		VI = 0 V, Vcc = 5 V	-	-	-5.0	μА
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5 V	30	50	167	kΩ
RfXCIN	Feedback resistance	XCIN		=	18	=	MΩ
VRAM	RAM hold voltage		During stop mode	2.0	=	=	V

NOTE

^{1.} Vcc = 4.2 to 5.5 V at Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.

Electrical Characteristics (2) [Vcc = 5 V] **Table 5.13** (Topr = -20 to 85° C (N version) / -40 to 85° C (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard		ł	Unit
Syllibol	Farameter		Condition	Min.	Тур.	Max.	Offic
Icc	Power supply current (Vcc = 3.3 to 5.5 V)	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	=	TBD	TBD	mA
	Single-chip mode, output pins are open, other pins		High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	П	TBD	-	mA
	are Vss	Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	=	TBD	TBD	μΑ
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	-	TBD	TBD	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	-	TBD	-	μА
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	TBD	μА
	L V F V V V V V V V V		High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	TBD	TBD	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	-	μА
		High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	-	μА	
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	TBD	TBD	μА
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	TBD	-	μА

Timing Requirements

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.14 XCIN Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(XCIN)	XCIN input cycle time	14	-	μS	
twh(xcin)	XCIN input "H" width	7	-	μS	
twl(xcin)	XCIN input "L" width	7	_	μS	

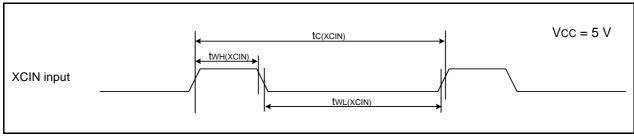


Figure 5.4 XCIN Input Timing Diagram when Vcc = 5 V

Table 5.15 TRAIO Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	100	=	ns	
twh(traio)	TRAIO input "H" width	40	=	ns	
tWL(TRAIO)	TRAIO input "L" width	40	-	ns	

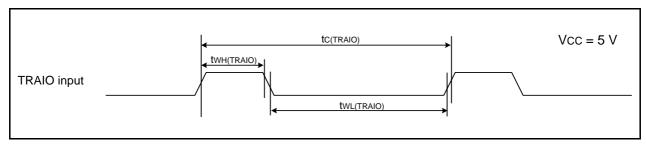


Figure 5.5 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.16 Serial Interface

Symbol	Parameter		Standard		
			Max.	Unit	
tc(CK)	CLKi input cycle time	200	-	ns	
tW(CKH)	CLKi input "H" width	100	-	ns	
tW(CKL)	CLKi input "L" width	100	-	ns	
td(C-Q)	TXDi output delay time	=	50	ns	
th(C-Q)	TXDi hold time	0	-	ns	
tsu(D-C)	RXDi input setup time	50	-	ns	
th(C-D)	RXDi input hold time	90	-	ns	

i = 0 or 2

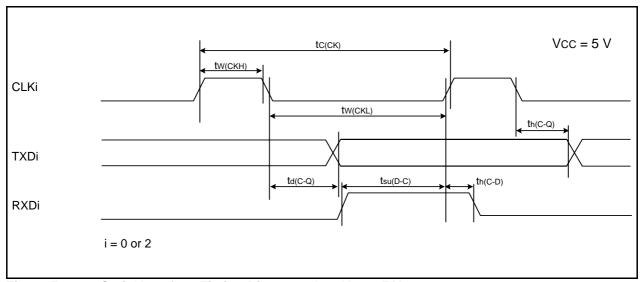


Figure 5.6 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.17 External Interrupt \overline{INTi} (i = 0 or 1) Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tW(INH)	ĪNTi input "H" width	250 ⁽¹⁾	-	ns	
tw(INL)	INTi input "L" width	250 ⁽²⁾	-	ns	

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

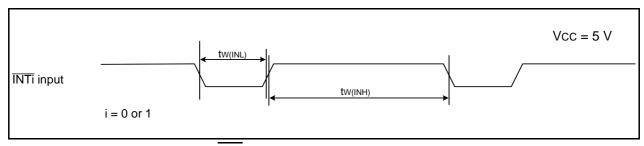


Figure 5.7 External Interrupt INTi Input Timing Diagram when Vcc = 5 V

Table 5.18 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter	Condition	9	Unit			
Symbol	Farameter		Condition	Min.	Тур.	Max.	Offic
Voн	Output "H" voltage		Iон = −1 mA	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage		IoL = 1 mA	-	=	0.5	V
VT+-VT-	Hysteresis	NT0, NT1, KI0, KI1, KI2, KI3, RXD0, RXD2, CLK0, CLK2		0.1	0.3	-	V
		RESET		0.1	0.4	=	V
Iн	Input "H" current		VI = 3 V, Vcc = 3 V	-	-	4.0	μΑ
lı∟	Input "L" current		VI = 0 V, Vcc = 3 V	=	-	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3 V	66	160	500	kΩ
RfXCIN	Feedback resistance	XCIN		-	18	-	MΩ
VRAM	RAM hold voltage		During stop mode	1.8	-	=	V

^{1.} Vcc =2.7 to 3.3 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.19 Electrical Characteristics (4) [Vcc = 3 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition	;	Standard	<u></u>	Unit
Symbol	Faranielei		Condition	Min.	Тур.	Max.	Utill
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode,	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	ı	TBD	TBD	mA
	output pins are open, other pins are Vss		High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	I	TBD	1	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	TBD	TBD	μА
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	-	TBD	TBD	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	-	TBD	-	μА
	Wa		High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	TBD	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	TBD	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	_	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	-	μА
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	TBD	TBD	μА
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	TBD	_	μА

Timing requirements

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C) [Vcc = 3 V]

Table 5.20 XCIN Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(XCIN)	XCIN input cycle time	14	=	μS	
twh(xcin)	XCIN input "H" width	7	-	μS	
twl(xcin)	XCIN input "L" width	7	-	μS	

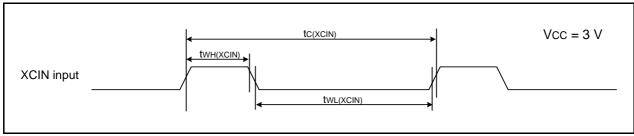


Figure 5.8 XCIN Input Timing Diagram when Vcc = 3 V

Table 5.21 TRAIO Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	300	=	ns	
tWH(TRAIO)	TRAIO input "H" width	120	=	ns	
tWL(TRAIO)	TRAIO input "L" width	120	-	ns	

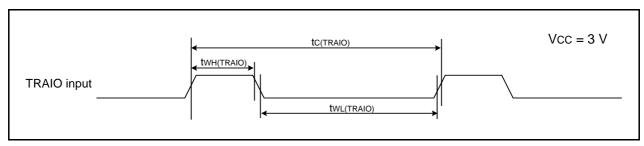


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.22 Serial Interface

Symbol	Parameter		Standard		
	Farameter	Min.	Max.	Unit	
tc(CK)	CLKi input cycle time	300	=	ns	
tW(CKH)	CLKi input "H" width	150	-	ns	
tW(CKL)	CLKi Input "L" width	150	-	ns	
td(C-Q)	TXDi output delay time	=	80	ns	
th(C-Q)	TXDi hold time	0	-	ns	
tsu(D-C)	RXDi input setup time	70	-	ns	
th(C-D)	RXDi input hold time	90	-	ns	

i = 0 or 2

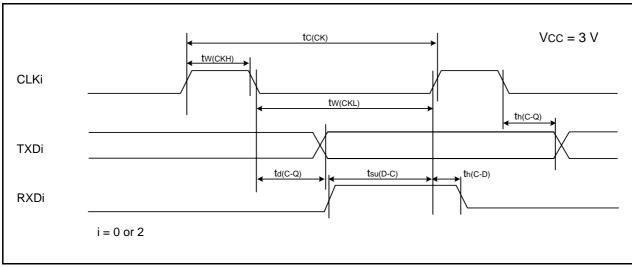


Figure 5.10 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.23 External Interrupt INTi (i = 0 or 1) Input

Symbol	Parameter		Standard		
	Symbol	i didilicici	Min.	Max.	Unit
	tw(INH)	ĪNTi input "H" width	380 ⁽¹⁾	-	ns
	tW(INL)	INTi input "L" width	380(2)	I	ns

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

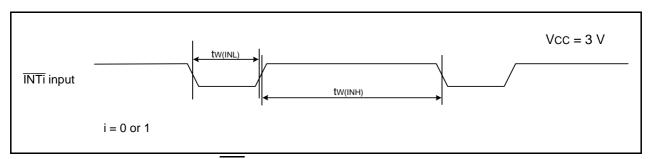


Figure 5.11 External Interrupt INTi Input Timing Diagram when Vcc = 3 V

Table 5.24 Electrical Characteristics (5) [Vcc = 2.2 V]

Symbol	Parameter	Condition	5	Unit			
Syllibol	Farameter		Condition	Min.	Тур.	Max.	Offic
Voн	Output "H" voltage		Iон = −1 mA	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage		IoL = 1 mA	-	=	0.5	V
VT+-VT-	Hysteresis	NT0, NT1, KI0, KI1, KI2, KI3, RXD0, RXD2, CLK0, CLK2		0.05	0.3	ı	V
		RESET		0.05	0.15	=	V
lін	Input "H" current		VI = 2.2 V	-	-	4.0	μΑ
lı∟	Input "L" current		VI = 0 V	=	-	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V	100	200	600	kΩ
RfXCIN	Feedback resistance	XCIN		-	35	-	MΩ
VRAM	RAM hold voltage		During stop mode	1.8	-	-	V

^{1.} VCC = 2.2 V at $T_{OPT} = -20 \text{ to } 85^{\circ}\text{C}$ (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.25 Electrical Characteristics (6) [Vcc = 2.2 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Parameter Condition			Standard	<u></u>	Unit
Symbol	Farameter		Condition	Min.	Тур.	Max.	Offic
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode,	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz No division	=	TBD	=	mA
	output pins are open, other pins are Vss		High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	ı	TBD	-	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	ı	TBD	TBD	μА
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	ı	TBD	TBD	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	-	TBD	_	μА
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	TBD	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	TBD	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	-	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	-	μА
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	TBD	TBD	μА
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	TBD	_	μА

Timing requirements

(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]

Table 5.26 XCIN Input

Symbol	Parameter		dard	Unit	
	Falameter	Min.	Max.	Offic	
tc(XCIN)	XCIN input cycle time	14	=	μS	
twh(xcin)	XCIN input "H" width	7	-	μS	
twl(xcin)	XCIN input "L" width	7	-	μS	

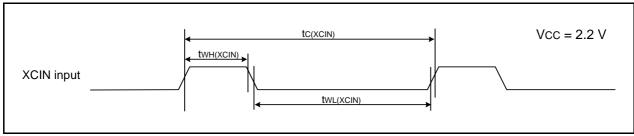


Figure 5.12 XCIN Input Timing Diagram when Vcc = 2.2 V

Table 5.27 TRAIO Input

Symbol	Parameter		Standard	
			Max.	Unit
tc(TRAIO)	TRAIO input cycle time	500	-	ns
twh(traio)	TRAIO input "H" width	200	=	ns
tWL(TRAIO)	TRAIO input "L" width	200	-	ns

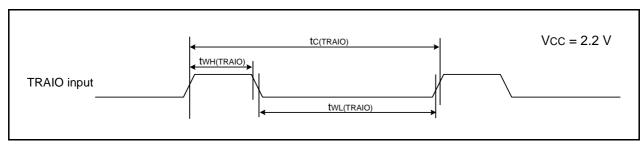


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5.28 Serial Interface

Symbol	Parameter		Standard	
	raiailietei	Min.	Max.	Unit
tc(CK)	CLKi input cycle time	800	-	ns
tW(CKH)	CLKi input "H" width	400	-	ns
tW(CKL)	CLKi input "L" width	400	-	ns
td(C-Q)	TXDi output delay time	-	200	ns
th(C-Q)	TXDi hold time	0	-	ns
tsu(D-C)	RXDi input setup time	150	-	ns
th(C-D)	RXDi input hold time	90	=	ns

i = 0 or 2

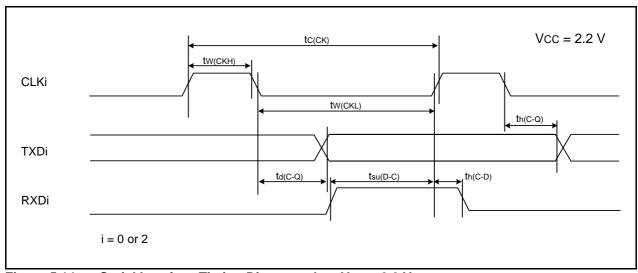


Figure 5.14 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.29 External Interrupt INTi (i = 0 or 1) Input

Symbol	Parameter	Stan	dard	Unit
	raianielei	Min.	Max.	Offic
tW(INH)	ĪNTi input "H" width	1000(1)	-	ns
tw(INL)	INTi input "L" width	1000(2)	1	ns

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

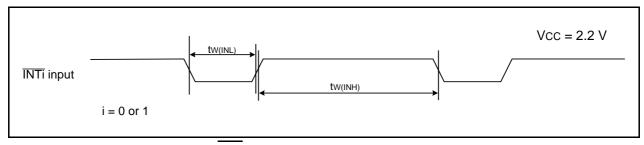


Figure 5.15 External Interrupt INTi Input Timing Diagram when Vcc = 2.2 V

5.2 R8C/2J Group

Table 5.30 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc	Supply voltage		-0.3 to 6.5	V
Vı	Input voltage		-0.3 to Vcc + 0.3	V
Vo	Output voltage		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	Topr = 25°C	500	mW
Topr	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
Tstg	Storage temperature		-65 to 150	°C

Table 5.31 Recommended Operating Conditions

Symbol	Parameter		Conditions		Unit		
Symbol	Paran	ietei	Conditions	Min.	Тур.	Max.	Unit
Vcc	Supply voltage			2.2	-	5.5	V
Vss	Supply voltage			-	0	-	V
VIH	Input "H" voltage			0.8 Vcc	-	Vcc	V
VIL	Input "L" voltage			0	_	0.2 Vcc	V
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)		_	_	-160	mA
IOH(sum)	Average sum output "H" current	Sum of all pins IOH(avg)		=	=	-80	mA
IOH(peak)	Peak output "H" current	All pins		-	=	-10	mA
IOH(avg)	Average output "H" current	All pins		-	-	-5	mA
IOL(sum)	Peak sum output "L" currents	Sum of all pins IOL(peak)		=	=	160	mA
IOL(sum)	Average sum output "L" currents	Sum of all pins IOL(avg)		=	=	80	mA
IOL(peak)	Peak output "L" currents	All pins		-	-	10	mA
IOL(avg)	Average output "L" current	All pins		_	-	5	mA
-	System clock		HRA01 = 0 Low-speed on-chip oscillator selected	=	125	=	kHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.7 V ≤ Vcc ≤ 5.5 V	=	-	8	MHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.2 V ≤ Vcc ≤ 5.5 V	_	-	4	MHz

- 1. Vcc = 2.2 to 5.5 V at $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. The typical values when average output current is 100 ms.

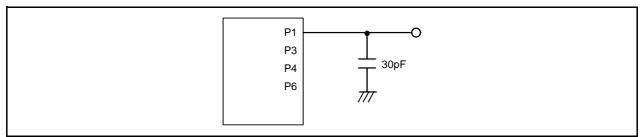


Figure 5.16 Ports P1, P3, P4, and P6 Timing Measurement Circuit

Table 5.32	Flash Memory	(Program ROM)	Electrical	Characteristics
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Cumbal	Doromotor	Conditions		Unit			
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Offic	
=	Program/erase endurance ⁽²⁾		100 ⁽³⁾	=	=	times	
_	Byte program time		-	50	400	μS	
_	Block erase time		-	0.4	9	S	
td(SR-SUS)	Time delay from suspend request until suspend		-	_	97 + CPU clock × 6 cycles	μS	
_	Interval from erase start/restart until following suspend request		650	_	_	μS	
_	Interval from program start/restart until following suspend request		0	_	_	ns	
=	Time from suspend until program/erase restart		=	-	3 + CPU clock × 4 cycles	μS	
_	Program, erase voltage		2.7	-	5.5	V	
-	Read voltage		2.2	-	5.5	V	
=	Program, erase temperature		0	=	60	°C	
=	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	_	-	year	

- NOTES:

 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60°C, unless otherwise specified.
 - 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

- However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

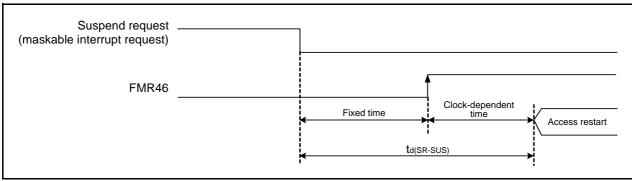


Figure 5.17 Time delay until Suspend

Table 5.33 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
Syllibol	Falameter	Condition	Min.	Тур.	Max.	Ullit
Vdet0	Voltage detection level		2.2	2.3	2.4	V
=	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	=	0.9	=	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		=	=	300	μ\$
Vccmin	MCU operating voltage minimum value		2.2	-	-	V

- 1. The measurement condition is Vcc = 2.2 V to 5.5 V and $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version).
- 2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.34 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
Syllibol	Faranteter	Condition	Min.	Тур.	Max.	Offic
Vdet1	Voltage detection level ⁽⁴⁾		2.70	2.85	3.00	V
_	Voltage monitor 1 interrupt request generation time ⁽²⁾		_	40	_	μS
=	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	=	0.6	=	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		-	_	100	μS

NOTES:

- 1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
- 4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.35 Voltage Detection 2 Circuit Electrical Characteristics

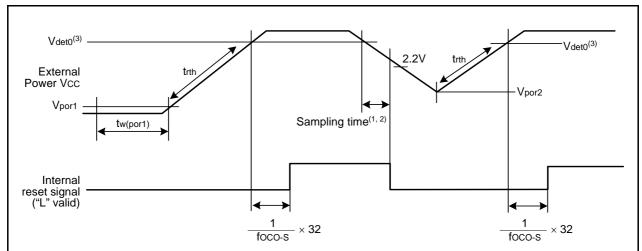
Symbol	Parameter	Condition	Standard			Unit
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet2	Voltage detection level		3.3	3.6	3.9	V
_	Voltage monitor 2 interrupt request generation time ⁽²⁾		_	40	_	μS
_	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	-	0.6	_	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		=	=	100	μS

- 1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
- 3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.36 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition		Standard	Unit	
Symbol	Falamete	Solidition		Тур.		Max.
Vpor1	Power-on reset valid voltage ⁽⁴⁾		_	-	0.1	V
Vpor2	Power-on reset or voltage monitor 0 reset valid voltage		0	_	Vdet0	V
trth	External power Vcc rise gradient(2)		20	_	_	mV/msec

- 1. The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. This condition (external power Vcc rise gradient) does not apply if Vcc ≥ 1.0 V.
- 3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
- 4. tw(por1) indicates the duration the external power Vcc must be held below the effective voltage (Vpor1) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30 s or more if -20°C ≤ Topr ≤ 85°C, maintain tw(por1) for 3,000 s or more if -40°C ≤ Topr < -20°C.</p>



- 1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
- 2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
- 3. Vdeto indicates the voltage detection level of the voltage detection 0 circuit. Refer to 6. Voltage Detection Circuit for details.

Figure 5.18 Reset Circuit Electrical Characteristics

Table 5.37 Comparator Electrical Characteristics

Symbol	Parameter	Condition		Standard		Unit
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vref	Internal reference voltage	$Vcc = 5.0 \pm 5.0 \text{ V}, Topr = 25^{\circ}C$	TBD	1.25	TBD	V
			TBD	1.25	TBD	V
CVREF	External reference voltage input range		-	TBD	TBD	V
VCMP1, VCMP2	External comparison voltage input range		_	TBD	TBD	V
=	Offset		=	TBD	TBD	mV
=	Response time		=	TBD	TBD	μS
_	Comparator self power consumption		=	TBD	TBD	μΑ

Table 5.38 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Cymphol	Parameter	Condition	Standard			Unit
Symbol		Condition	Min.	Тур.	Max.	Unit
fOCO-F	High-speed on-chip oscillator frequency temperature • supply voltage dependence	Vcc = 4.75 V to 5.25 V 0° C \leq Topr \leq 60° C ⁽²⁾	7.76	8	8.24	MHz
		Vcc = 2.7 V to 5.5 V -20° C \leq Topr \leq 85 $^{\circ}$ C ⁽²⁾	7.68	8	8.32	MHz
		Vcc = 2.7 V to 5.5 V -40°C \leq Topr \leq 85°C ⁽²⁾	7.44	8	8.32	MHz
		Vcc = 2.2 V to 5.5 V -20° C \leq Topr \leq 85 $^{\circ}$ C ⁽²⁾	TBD	8	TBD	MHz
		Vcc = 2.2 V to 5.5 V -40°C \le Topr \le 85°C(2)	TBD	8	TBD	MHz

NOTES:

- 1. The measurement condition is $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.
- 2. These standard values show when the HRA1 register is set to the value before shipment and the HRA2 register is set to 00h.

Table 5.39 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Svmbol	Parameter	Condition		Unit		
Symbol	r alametei	Condition	Min.	Тур.	Max.	Offic
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
_	Oscillation stability time		-	10	100	μS
_	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	_	15	1	μА

NOTE:

1. Vcc = 2.2 to 5.5 V, Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.

Table 5.40 Power Supply Circuit Timing Characteristics

Svmbol	Parameter	Condition	Standard			Unit
Syllibol	r alametel	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	=	TBD	μS
td(R-S)	STOP exit time ⁽³⁾		-	-	TBD	μS

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = 25°C.
- 2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
- 3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

^{1.} The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.41 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Doro	meter	Condition	S	tandard		Unit
Symbol	Faia	imeter	Condition	Min.	Тур.	Max.	Offic
Voн	Output "H" voltage		Iон = −5 mA	Vcc - 2.0	_	Vcc	V
			IOH = -200 μA	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage		IoL = 5 mA	=	-	2.0	V
			IoL = 200 μA	=	-	0.45	V
VT+-VT-	Hysteresis	INT0, INT1, KIO, KI1, KI2, KI3, RXD0, CLK0		0.1	0.5	-	V
		RESET		0.1	1.0	-	V
Іін	Input "H" current	-	VI = 5 V, Vcc = 5 V	-	_	5.0	μА
lı∟	Input "L" current		VI = 0 V, Vcc = 5 V	=	-	-5.0	μА
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5 V	30	50	167	kΩ
VRAM	RAM hold voltage		During stop mode	2.0	_	-	V

^{1.} Vcc = 4.2 to 5.5 V at $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.

Table 5.42 Electrical Characteristics (2) [Vcc = 5 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Cumbal	Parameter		Condition	Standard			Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
Icc	Power supply current (Vcc = 3.3 to 5.5 V)	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	TBD	TBD	mA
	Single-chip mode, output pins are	but pins are nother pins	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	TBD	_	mA
	are Vss	Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	_	TBD	TBD	μА
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	TBD	μΑ
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	TBD	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	-	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	TBD	_	μА
		Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	TBD	TBD	μΑ
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	TBD	-	μА

Timing Requirements

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.43 TRAIO Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	100	-	ns	
twh(traio)	TRAIO input "H" width	40	-	ns	
twl(traio)	TRAIO input "L" width	40	-	ns	

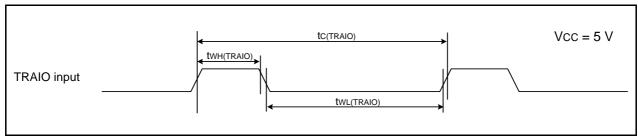


Figure 5.19 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.44 Serial Interface	Table	5.44	Serial Interfa	ce
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Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(CK)	CLK0 input cycle time	200	-	ns	
tW(CKH)	CLK0 input "H" width	100	-	ns	
tW(CKL)	CLK0 input "L" width	100	-	ns	
td(C-Q)	TXD0 output delay time	-	50	ns	
th(C-Q)	TXD0 hold time	0	-	ns	
tsu(D-C)	RXD0 input setup time	50	=	ns	
th(C-D)	RXD0 input hold time	90	=	ns	

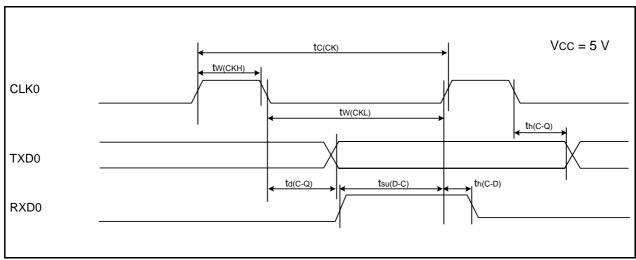


Figure 5.20 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.45 External Interrupt INTi (i = 0 or 1) Input

Symbol	Parameter	Stan	dard	Unit
Symbol	Faranielei		Max.	Offic
tW(INH)	ĪNTi input "H" width	250 ⁽¹⁾	-	ns
tW(INL)	ĪNTi input "L" width	250(2)	-	ns

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

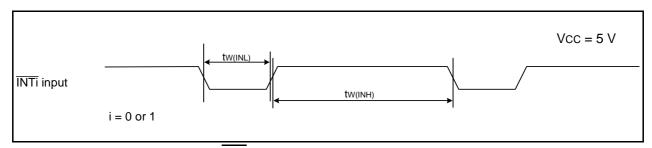


Figure 5.21 External Interrupt INTi Input Timing Diagram when Vcc = 5 V

Table 5.46 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parar	motor	Condition	5	Standard		Unit
Symbol	Falai	neter	Condition	Min.	Тур.	Max.	Offic
Vон	Output "H" voltage		Iон = −1 mA	Vcc - 0.5	=	Vcc	V
Vol	Output "L" voltage		IOL = 1 mA	=	=	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, KI0, KI1, KI2, KI3, RXD0, CLK0		0.1	0.3	-	V
		RESET		0.1	0.4	_	V
Iн	Input "H" current		VI = 3 V, Vcc = 3 V	=	=	4.0	μΑ
lıL	Input "L" current		VI = 0 V, Vcc = 3 V	=	=	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3 V	66	160	500	kΩ
VRAM	RAM hold voltage		During stop mode	1.8	-	-	V

^{1.} Vcc = 2.7 to 3.3 V at Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.

Table 5.47 Electrical Characteristics (4) [Vcc = 3 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

			<u> </u>				
Symbol	Parameter		Condition			t	Unit
Cyrribor	Tarameter		Condition	Min.	Тур.	Max.	Oill
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode,	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	TBD	TBD	mA
	output pins are open, other pins are Vss		High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	TBD	=	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	=	TBD	TBD	μΑ
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	TBD	TBD	μΑ
		High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	TBD	TBD	μΑ	
			High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	TBD	-	μА
Stop mode		High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	TBD	-	μА	
	Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	TBD	TBD	μА	
		Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	TBD	_	μА	

Timing requirements

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C) [Vcc = 3 V]

Table 5.48 TRAIO Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time		-	ns	
twh(traio)	TRAIO input "H" width		-	ns	
twl(traio)	TRAIO input "L" width	120	-	ns	

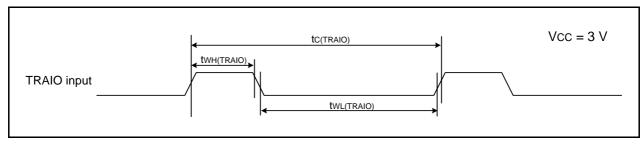


Figure 5.22 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.49 Serial Interface	Table	5.49	Serial	Interface
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Symbol	Parameter		Standard		
Syllibol			Max.	Unit	
tc(CK)	CLK0 input cycle time		-	ns	
tW(CKH)	CLK0 input "H" width	150	-	ns	
tW(CKL)	CLK0 Input "L" width		-	ns	
td(C-Q)	TXD0 output delay time		80	ns	
th(C-Q)	TXD0 hold time		-	ns	
tsu(D-C)	RXD0 input setup time		=	ns	
th(C-D)	RXD0 input hold time		=	ns	

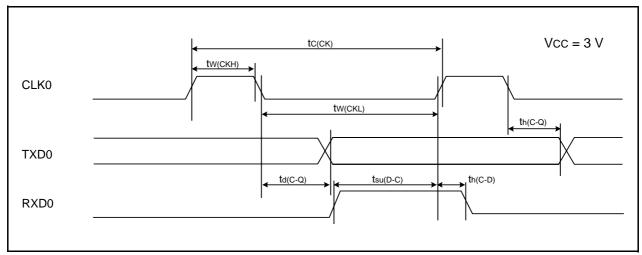


Figure 5.23 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.50 External Interrupt INTi (i = 0 or 1) Input

Symbol	Symbol Parameter		Standard		
Symbol			Max.	Unit	
tW(INH)	INTi input "H" width	380(1)	-	ns	
tW(INL)	INTi input "L" width	380(2)	-	ns	

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

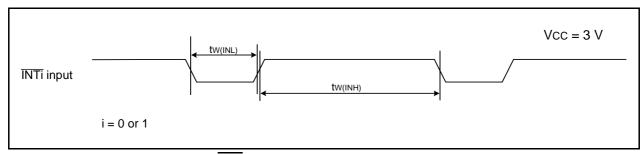


Figure 5.24 External Interrupt INTi Input Timing Diagram when Vcc = 3 V

Table 5.51 Electrical Characteristics (5) [Vcc = 2.2 V]

Cumbal	Parameter	Condition	Standard			Unit	
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
Vон	Output "H" voltage		Iон = −1 mA	Vcc - 0.5	ı	Vcc	V
Vol	Output "L" voltage		IoL = 1 mA	-		0.5	V
VT+-VT-	Hysteresis	NT0, NT1, KI0, KI1, KI2, KI3, RXD0, CLK0		0.05	0.3	-	V
		RESET		0.05	0.15	-	V
Iн	Input "H" current		VI = 2.2 V	-	1	4.0	μА
lıL	Input "L" current		VI = 0 V	=	=	-4.0	μА
RPULLUP	Pull-up resistance		VI = 0 V	100	200	600	kΩ
RfXCIN	Feedback resistance	XCIN		-	35	_	МΩ
VRAM	RAM hold voltage		During stop mode	1.8	ii ii	-	V

^{1.} VCC = 2.2 V at $T_{OPT} = -20 \text{ to } 85^{\circ}\text{C}$ (N version) / $-40 \text{ to } 85^{\circ}\text{C}$ (D version), unless otherwise specified.

Table 5.52 Electrical Characteristics (6) [Vcc = 2.2 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

		·					
Symbol	Parameter		Condition Standard				Unit
Cymbol	rarameter		Condition	Min.	Тур.	Max.	0
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode,	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	TBD	-	mA
	output pins are open, other pins are Vss		High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	TBD	-	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	TBD	TBD	μΑ
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	TBD	TBD	μΑ
		High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	TBD	TBD	μΑ	
			High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	TBD	-	μА
		High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	TBD	-	μА	
	Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	TBD	TBD	μА	
		Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	TBD	-	μА	

Timing requirements

(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at $Topr = 25^{\circ}C$) [Vcc = 2.2 V]

Table 5.53 TRAIO Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time		-	ns	
twh(traio)	TRAIO input "H" width		-	ns	
twl(traio)	TRAIO input "L" width	200	-	ns	

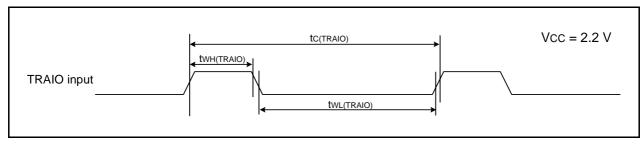


Figure 5.25 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5	.54	Serial	Interface
Iabic	.77	Jenai	IIIICIIacc

Symbol	Parameter		Standard		
Syllibol			Max.	Unit	
tc(CK)	CLK0 input cycle time		-	ns	
tW(CKH)	CLK0 input "H" width	400	=	ns	
tW(CKL)	CLK0 input "L" width		=	ns	
td(C-Q)	TXD0 output delay time		200	ns	
th(C-Q)	TXD0 hold time		=	ns	
tsu(D-C)	RXD0 input setup time		=	ns	
th(C-D)	RXD0 input hold time		=	ns	

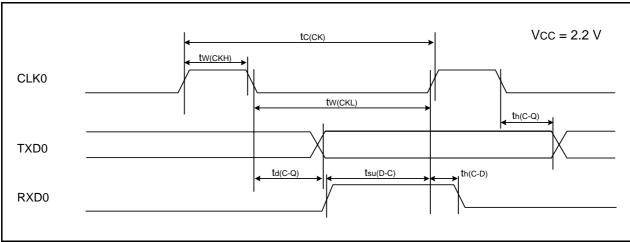


Figure 5.26 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.55 External Interrupt INTi (i = 0 or 1) Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tw(INH)	ĪNTi input "H" width	1000(1)	-	ns	
tw(INL)	INTi input "L" width	1000 ⁽²⁾	-	ns	

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

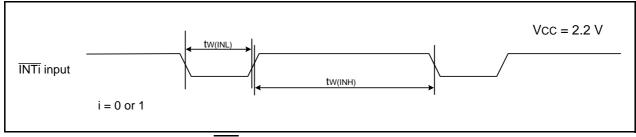
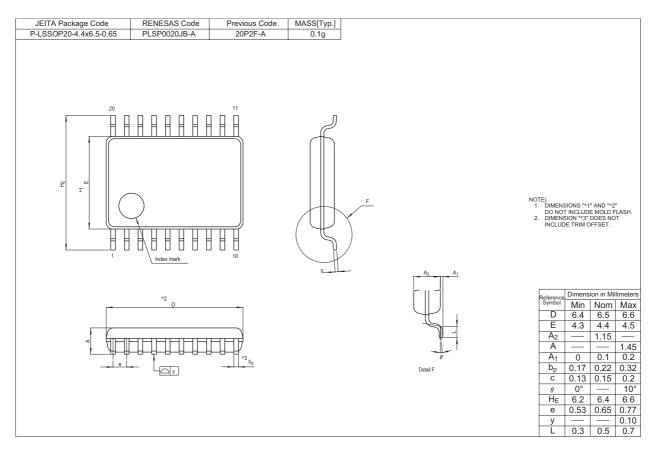


Figure 5.27 External Interrupt INTi Input Timing Diagram when Vcc = 2.2 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Technology website.



REVISION HISTORY	R8C/2H Group, R8C/2J Group Datasheet
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Rev.	Date	Description			
		Page	Summary		
0.01	Jun 18, 2007	_	First Edition issued		
0.10	Jul 20, 2007	20	Table 4.2: 0038h After reset; "0000X010b" → "1000X010b", "0100X011b" → "1100X011b"		
		31 to 64	5. Electrical Characteristics added		

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